

3D-NUMERICAL SIMULATION OF NANOSCALE Pi GATE SOI N- MOSFET TRANSISTOR WITH HIGH-k DIELECTRIC AND GRDUAL DOPING OF THE CHANNEL

Fatima Zohra Rahou

A.Guen Bouazza

B. Bouazza

Reasearch Unit of Materials and Renewable Energies,
Electrical and Electronic Engineering Department, Faculty of Technology,
University of Abou-Bekr Belkaid, Tlemcen, Algeria

Abstract

The Pi gate SOI MOSFET is a very good candidate for future VLSI due to its simple architecture and better performance: better control over short channel effects (SCEs) and reduced power dissipation due to reduced gate leakage currents.

In this paper, we present the results of a 3D-numerical simulation of nanoscale Pi gate SOI MOSFET transistor. 3D-device structure, based on technology SOI [Silicon-On-Insulator] is described and simulated by using SILVACO TCAD tools.

As the oxide thickness scales below 2 nm, leakage currents due to tunneling increase drastically, leading to high power consumption and reduced device reliability. Replacing the silicon dioxide gate dielectric with a high- κ material allows increased gate capacitance without the associated leakage effects.

To improve also the performance of the transistor Pi gate SOI MOSFET and to reduce the parasitic effects of to the structure SOI, we introduced the gradual doping of the channel.

Keywords: Multi-gate SOI MOSFET, Pi-gate SOI MOSFET, high-k dielectric, gradual doping of the channel, SILVACO software

Introduction:

With down-scaling of CMOS, the short-channel effects (SCEs) which are caused by the decreasing gate control over the channel are among the most important challenges in the semiconductor industry. In order to suppress the

SCEs, new structures, such as multiple-gate silicon-on insulator MOSFETS, have been proposed due to their ability to overcome several limitations like low speed and reduced short-channel effects (SCEs) (J.P.coligne, 2004). The most important types of multiple-gate SOI MOSFET devices are summarized in Figure 1, represented by the number of gates around the channel.

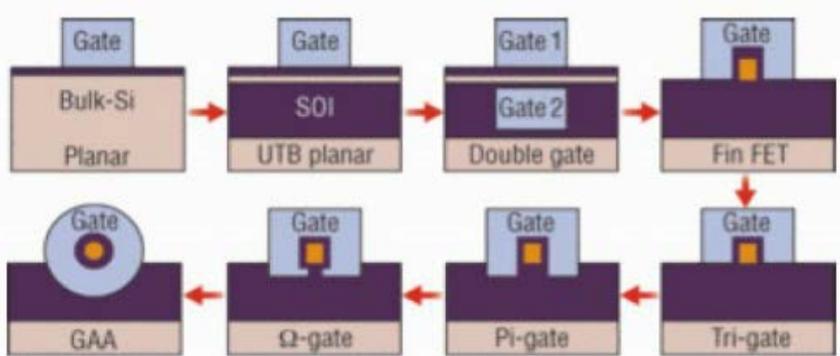


Fig. 1: Progress of the MOSFET Technology through multiple-gates (N. Gupta and all. 2014).

Of all SOI MOSFET structures, triple-gate transistors are very promising because it combines good sub threshold characteristics with high on-currents and are considered to be very good alternatives to planar devices.

In this paper, we chose the Pi gate SOI MOSFET transistor because the Pi-gate has great potential to replace the current used devices do to its geometry that is part-way between triple-gate and quadruple gate devices (J.T. Park and all.,2001), (F. J. G. Ruiz and all.,2007). The gate goes down into the buried oxide, allowing a more effective control of the electrostatics in the channel region and shielding it from the electric-field lines originated in the drain when the width of the devices is small enough (J. Frei and all.,2004), (F. Daugé and all.,2004).

Unlike the double-gate or a gate-all-around structure, however, the Pi-gate SOI MOSFET can readily be manufactured, since it merely requires the addition of a masking and an RIE buried oxide etch step to a conventional SOI CMOS fabrication process (Fig.2).

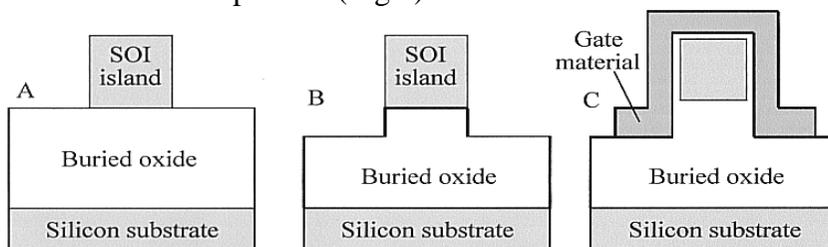


Fig. 2: Basic Pi-gate fabrication steps (cross section): A: silicon island patterning; B: shallow buried oxide RIE; C: gate oxide growth and gate material deposition and patterning (J. T. Park and all. 2002).

Numerical analysis

Numerical simulation is an extremely helpful tool for detailed investigation of physical phenomena, which determine electrical characteristics of semiconductor devices. Simulation results we present in this study had been obtained using Atlas Silvaco Software (Silvaco, 1995).

The starting point for our simulations is a basic structure represented in Fig.3. The different parameters of our structure are assumed as follows:

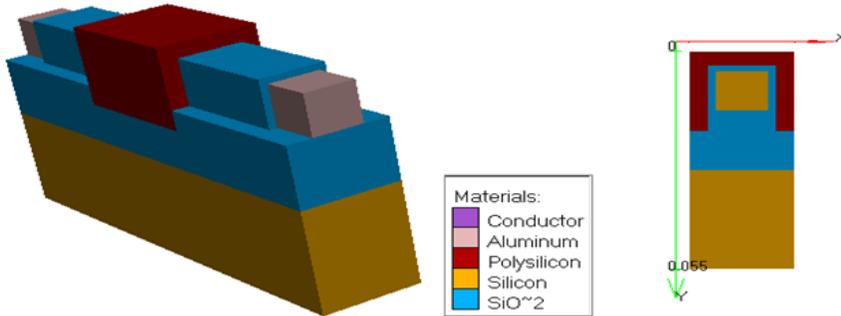


Fig. 3: Pi gate SOI N- MOSFET 3-D structure and cross-sectional view.

Typical values of the transistor parameters used in these simulations are shown in Table 1.

Table 1: Parameters of Pi gate SOI N -MOSFET transistor

Symbol	Designation	Value
N_A	Substrate concentration	$5 \times 10^{17} [\text{cm}^{-3}]$
N_D	Drain and Source concentration	$5 \times 10^{21} [\text{cm}^{-3}]$
L_G	Gate length	30 [nm]
T_{OX}	Latéral oxide thickness	1.5 [nm]
W_{FIN}	Width FIN	10[nm]
H_{FIN}	Height FIN	10[nm]
T_{BOX}	Buried oxide thickness	15[nm]
$T_{Substrate}$	Substrate thickness	25[nm]

The simulated transfer and output characteristics, transconductance, sub threshold voltage and leakage current of our basic structure are plotted respectively in Figs 4,5,6,7 and 8.

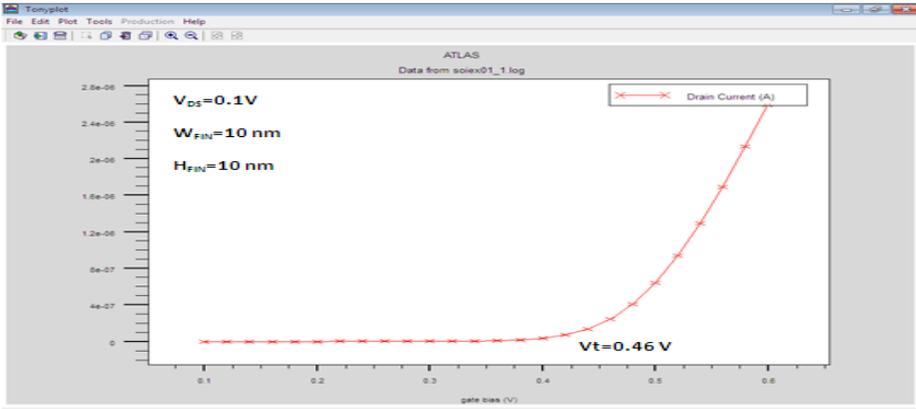


Fig. 4: Simulated transfer characteristic $I_{DS}-V_{GS}$ of Pi gate SOI N- MOSFET transistor.

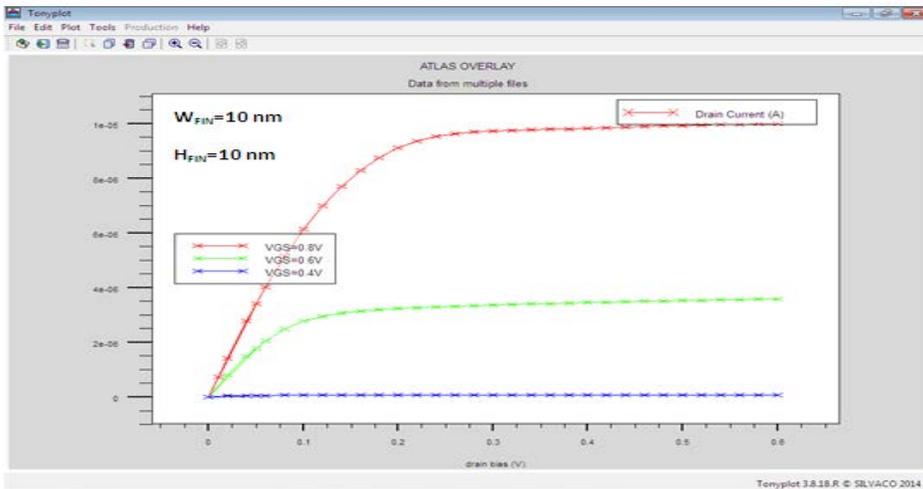


Fig. 5: Simulated Output characteristics $I_{DS}-V_{DS}$ of the Pi gate SOI N-MOSFET transistor.

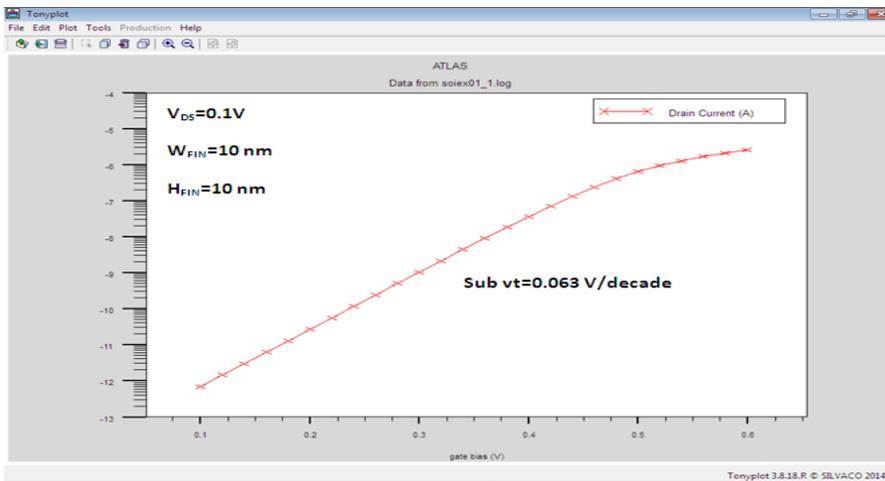


Fig.6: $I_{DS}-V_{GS}$ sub threshold voltage of Pi gate SOI N-MOSFET transistor.

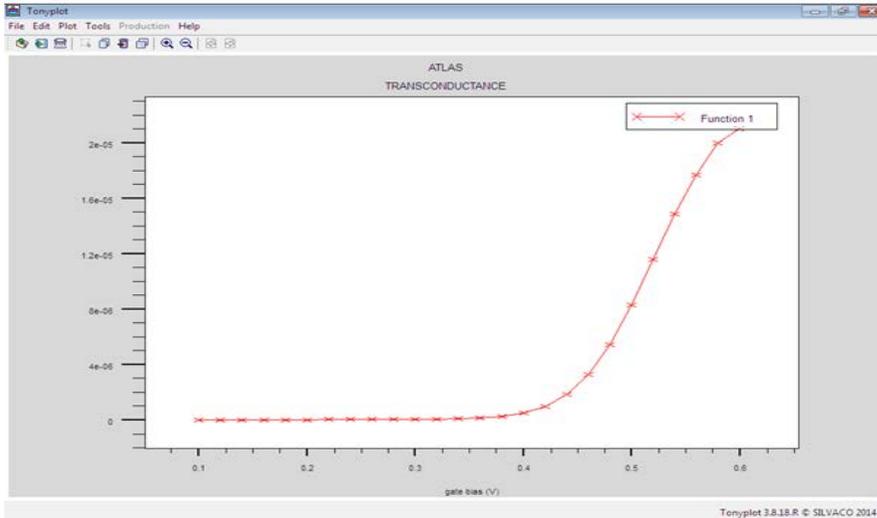


Fig. 7: Transconductance of Pi gateSOI N-MOSFET transistor.

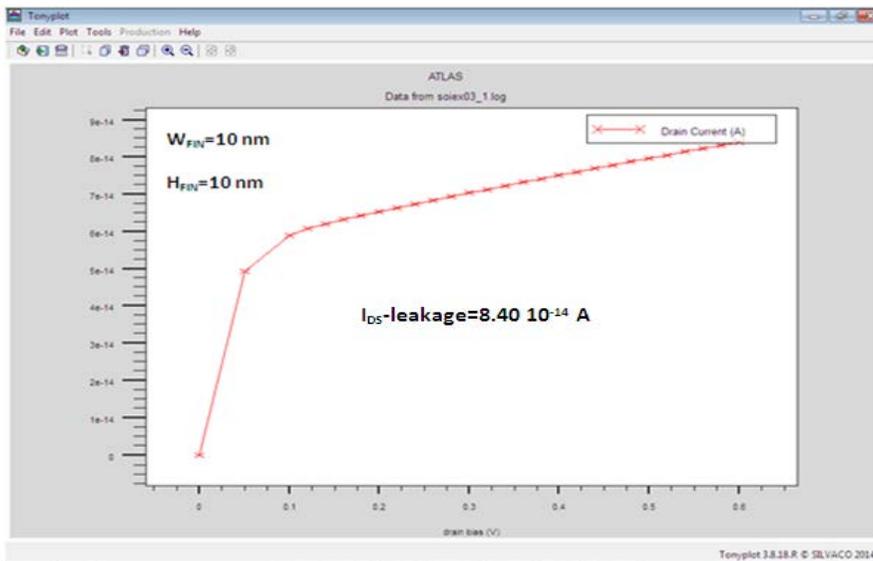


Fig. 8: Leakage current output of Pi gate SOI N- MOSFET transistor.

The DIBL [Drain-Induced Barrier Lowering] is a very significant parameter which translates the boring effect on the short channels; it is obtained by carrying out the difference on threshold voltage for two voltages drain, a first rather high (0.4V) and the second is very weak (0.05V).

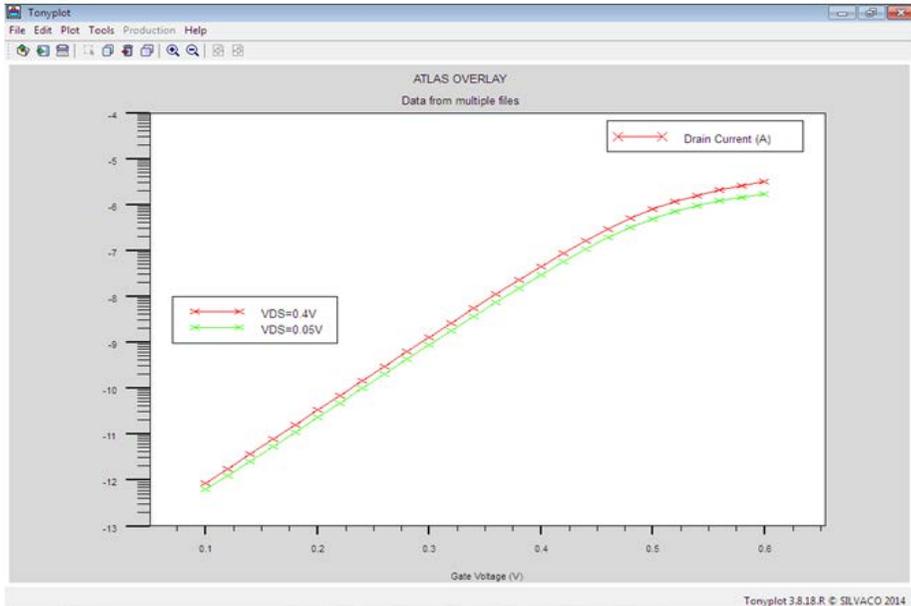


Fig. 9: DIBL effect in Pi gate SOI N- MOSFET transistor.

$$DIBL = \frac{V_{th}|_{V_{ds2}} - V_{th}|_{V_{ds1}}}{V_{ds2} - V_{ds1}} = 0.48$$

As transistors have decreased in size, the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance and thereby drive current, raising device performance.

High- κ dielectrics are used in semiconductor manufacturing processes where they are usually used to replace a silicon dioxide gate dielectric or another dielectric layer of a device.

To reduce the parasitic effects of to the structure SOI, we introduced the gradual doping of the channel.

To improve the performance of our transistor Pi gate SOI N-MOSFET, we replaced the silicon dioxide gate dielectric by high- κ gate dielectrics: the La_2O_3 which the permittivity equal to 30.

Introducing high permittivity insulator requires the use of a metal instead of Polysilicon gate, in our structure, we use Aluminum metal.

In addition to that, we introduce a gradual doping channel, in the structure shown below, the channel doping varies between 5×10^{16} and 5×10^{17} atoms / cm^3 .

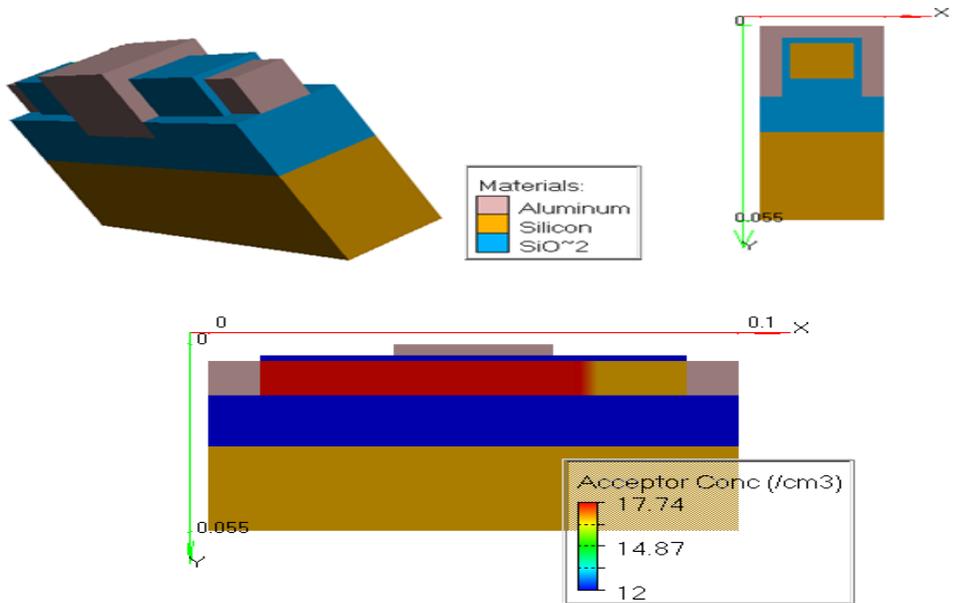


Fig. 10: Pi gate SOI N- MOSFET 3-D structure, cross-sectional view and cross-sectional view with gradual doping.

Figs 11, 12, 13, 14, 15 and 16 present respectively transfer and output characteristics, sub threshold voltage, transconductance, leakage current and DIBL effect in Pi gate SOI N- MOSFET transistor.

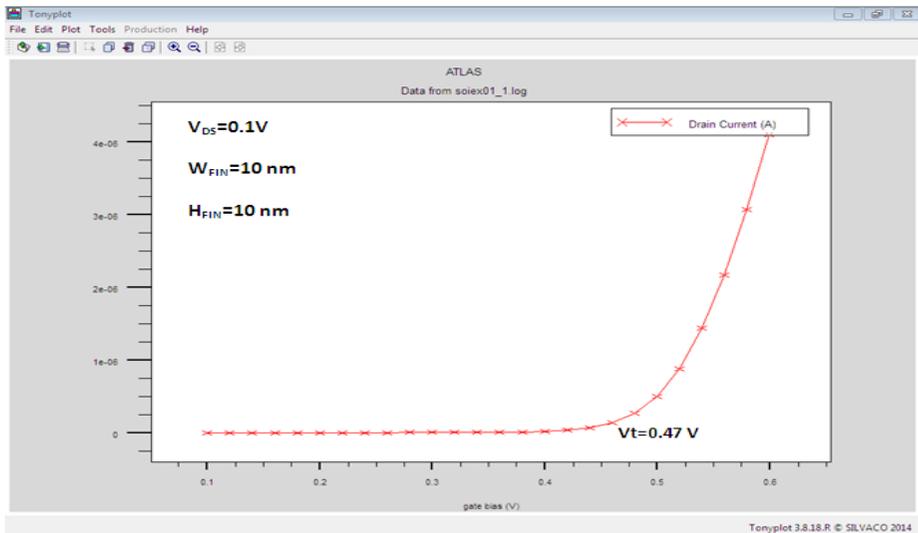


Fig.11: Simulated transfer characteristic $I_{DS}-V_{GS}$ of Pi gate SOI N- MOSFET transistor.

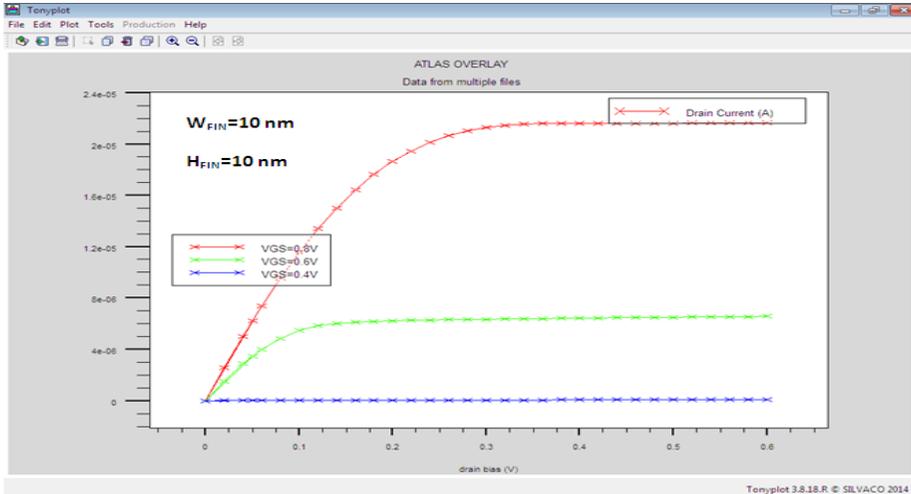


Fig.12: Simulated Output characteristics $I_{DS}-V_{DS}$ of the Pi gate SOI N-MOSFET transistor.

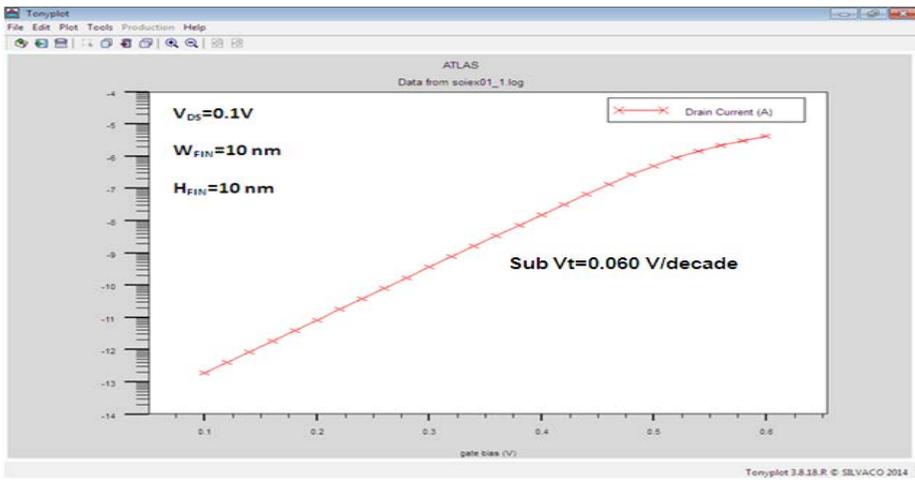


Fig.13: $I_{DS}-V_{GS}$ sub threshold voltage of Pi gate SOI N-MOSFET transistor.

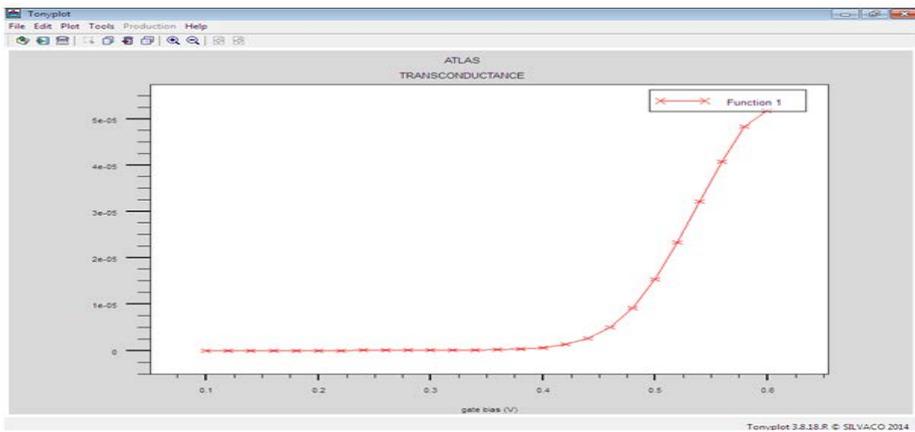


Fig.14: Transconductance of Pi gate SOI N-MOSFET transistor.

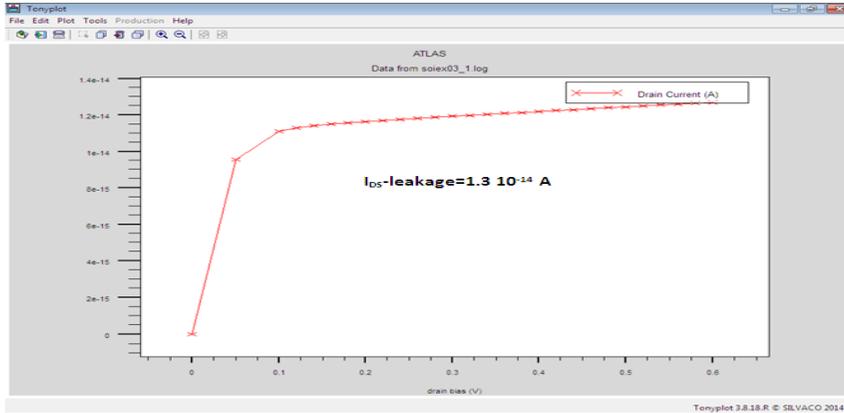


Fig.15: Leakage current output of Pi gate SOI N- MOSFET transistor

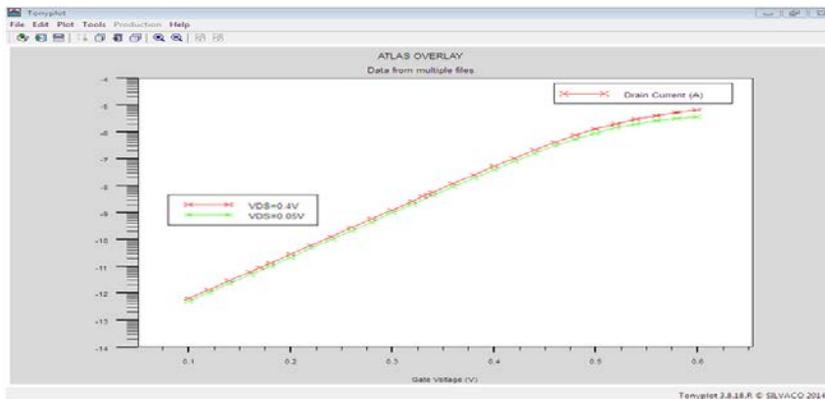


Fig.16: DIBL effect in Pi gate SOI N- MOSFET transistor.

$$DIBL = \frac{V_{th}|V_{ds2} - V_{th}|V_{ds1}}{V_{ds2} - V_{ds1}} = 0.4$$

In these figures we can clearly see the improvement of the performance of the transistor compared to the initial structure.

The following table provides a comparison between the simulation results of the pi gate SOI N -MOSFET transistor with silicon dioxide gate (SiO₂) and without gradual doping channel and the pi gate SOI N-MOSFET transistor with high-κ gate dielectrics (La₂O₃) with gradual doping channel.

	Pi gate SOI N-MOSFET with SiO ₂ dielectric and without gradual doping channel	Pi gate SOI N-MOSFET with La ₂ O ₃ dielectric and with gradual doping channel
V _t [V]	0.46	0.47
I _{DSAT} [A] (V _{GS} =0.8V)	10 ⁻⁵	2.2 10 ⁻⁵
sub threshold voltage [V/decade]	0.063	0.60
Transconductance gm-max [A/V]	2.2 10 ⁻⁵	5.2 10 ⁻⁵
I _{DS} -Leakage current [A]	8.40 10 ⁻¹⁴	1.3 10 ⁻¹⁴
DIBL	0.48	0.4

Conclusion:

From these simulations results of the structure of the pi gate SOI N-MOSFET transistor we can see the effect of replacing silicon dioxide gate (SiO_2) by high- κ gate dielectrics (La_2O_3) with introduced the gradual doping of the channel.

The implementation of high- κ gate dielectrics is one of several strategies developed to allow further miniaturization of microelectronic components.

Pi gate SOI N-MOSFET with high- κ dielectrics and gradual doping of the channel gives improvements in almost every respect such as improved threshold-voltage, transconductance, saturation current, sub threshold voltage, leakage current and DIBL effect. Better reduction of SCEs and an improvement in the device reliability has been observed through the simulation results.

References:

J. P. Colinge, "Multiple-gate SOI MOSFETs," *Solid State Electronic*, v. 48, n. 6, pp. 897–905, 2004.

Neeraj Gupta; A.K. Raghav; Alok K. Kushwaha. A Study on Multi Material Gate All Around SOI MOSFET, IJTEL, ISSN: 2319-2135, VOL.3, NO.3, JUNE 2014.

J. T. Park, J. P. Coling and C. H. Diaz, "Pi-Gate SOI MOSFET", *IEEE Electron Device Letters*, v. 22, n. 8, pp. 405- 406, 2001.

F. J. G. Ruiz, A. Godoy, F. Gámiz, C. Sampedro and L. Donetti, "A Comprehensive Study of the Corner Effects in Pi- Gate MOSFETs Including Quantum Effects", *IEEE Transactions on Electron Device*, v. 54, n. 12, pp. 3369-3377, 2007.

J. Frei, C. Johns, A. Vazquez, W. Xiong, C. R. Cleavelin, T. Schulz, N. Chaudhary, G. Gebara, J. R. Zaman, M. Gostkowski, K. Matthews and J. P. Colinge, "Body Effect in Tri- and Pi- Gate SOI MOSFETs", *IEEE Electron Device Letters*, v. 25, n. 12, pp. 813-815, 2004.

F. Dauge, J. Pretet, S. Cristoloveanu, A. Vandooren, L. Mathew, J. Jomaah and B. Y. Nguyen, "Coupling effects and channels separation in FinFETs" *Solid State Electronic*, v. 48, pp. 535–542, 2004.

Jong-Tae Park, *Member, IEEE*, and Jean-Pierre Colinge, *Fellow, IEEE*, "Multiple-Gate SOI MOSFETs: Device Design Guidelines", *IEEE TRANSACTIONS ON ELECTRON DEVICES*, VOL. 49, NO. 12, DECEMBER 2002.

SILVACO, ATLAS User's Manual, Ver. 4.0, June 1995.