DEVELOPMENT OF THE DATA TRANSFERING SYSTEM USING SOC

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Abstract

The aim of work was analyzes of SoC and design of the wireless data transfer system.

The modern industrial control systems and technologies connected to design of data transfering systems are analyzed. Advantages of implementation of such systems on FPGA are described. The Dispatching automation system "KARJER" is described. System controls navigational parameters (coordinates, speed) of vehicles as well as condition of onboard equipment like truck body load and amount of fuel left in its fuel tank. Information gets collected using GPS technologies.To improve the parameters of this system for determination of objects positions it was proposed to receive data from several sources and send them to the user by means of GSM modules and short messages of the SMS. Design of data transfering system is considered. It constructs of two serial input-output ports to exchange data with GPS and GSM modules and processor. For programming and simulation of the main blocks of the transfering system the following software are used: Xilinx ISE Design Suite; Aldec Active HDL; Quartus II Web Edition. To develop and test the board Xilinx Spartan-3E Starter Kit and software Xilinx ISE Design suite are used. Results of HDL simulation of developed system are shown. The developed controller can be used as basic for development of industrial devices of specialized assignment; the received results also can be used as a bright example for the students training.

Keywords: System on a chip, reciever, transmitter, FPGA, HDL - model

Introduction

One of principal directions of systems on a chip (SoC) applications is developing of special purpose monitoring devices. Depending on assignment the SoC can operate with digital, analog, analog-to-digital signals, and also radio frequencies band. As a rule, similar devices are applied in portable and embeddable systems. The market of similar systems permanently grows. It means relevance of their development, and also research of methods design and interaction. SoC can be implemented on FPGA. This approach has the following advantages: smaller costs of development and prototype creation; multiple adjustment of the project; use of well checked serial chips; possibility for debugging and testing "in parts"; possibility to extension of the device function; support the principle of reconfiguration [1].

The aim of work was analyzes of SoC and design of the wireless data transfer system.

Thereby assigned and solved the following tasks:

- the analysis of the modern industrial control systems and technologies connected to design of data transfering systems;
- the analysis of algorithms of reconfigurable systems creation, including standard SoC;
- development of the data transfering system using SoC;
- simulation of the developed system on VHDL.

Main Text

As an example of modern industrial control systems the Dispatching automation system "KARJER" [2] is analyzed (fig.1).

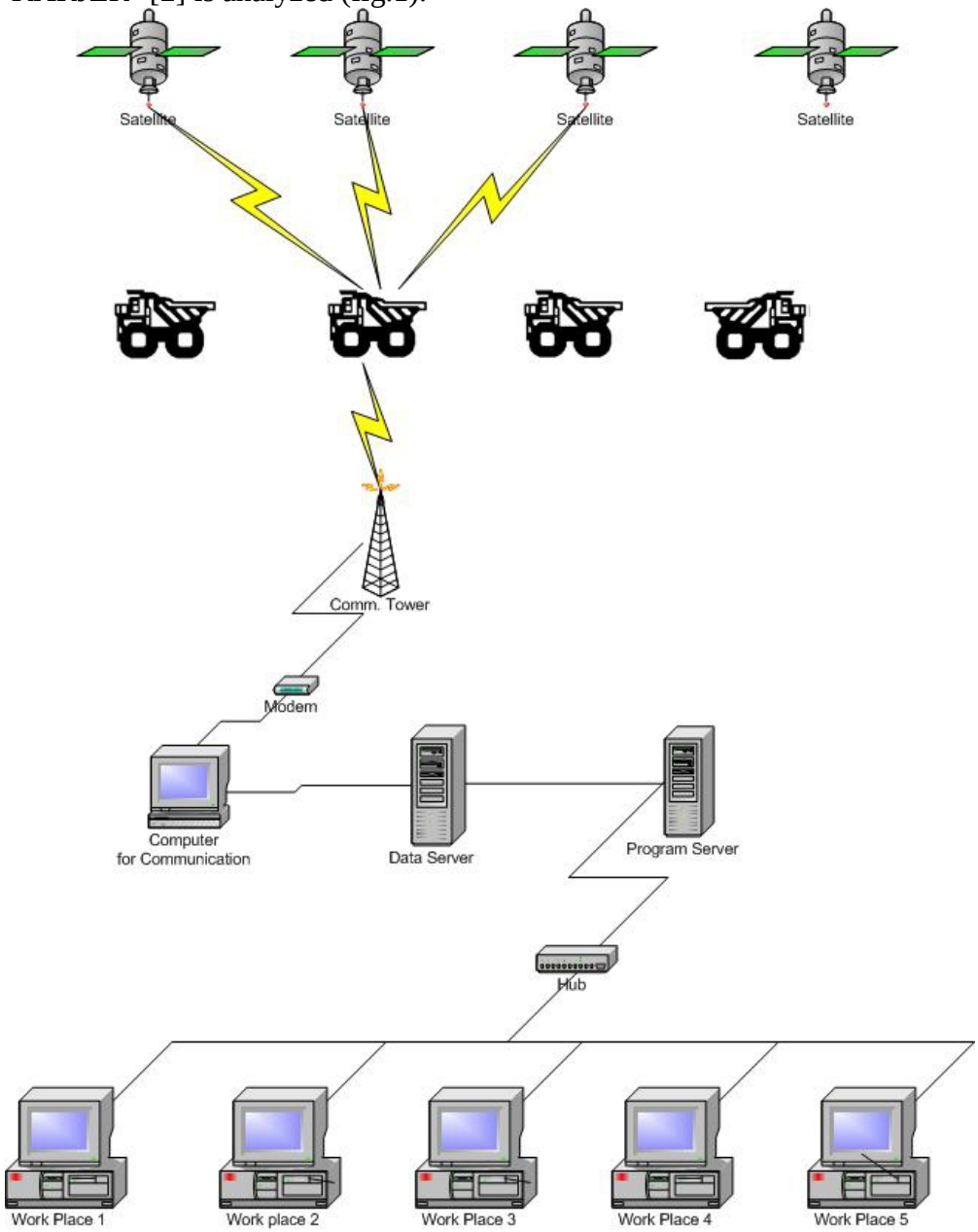

Fig.1. Structure of Dispatching automation system "KARJER"

It solves different tasks in the fields of control and management of mining transportation complex as well as optimizes quarrying process. System updates dispatchers and management staff with information on current condition of vehicles, number of trips completed, amount of cargo transported and fuel consumed, and other parameters that characterize freight flow activities. System controls navigational parameters (coordinates, speed) of vehicles as well as condition of onboard equipment like truck body load and amount of fuel left in its fuel tank. Information gets collected using GPS technologies (Global Positioning System). Data gets transferred in the dispatching center automatically in digital format over VHF radio channel. System ensures operative graphical representation of collected information on remote user terminals in corporate dispatching center and stores it for further recording and analysis.

The main of onboard controller is data transmission systems. To improve the parameters of Dispatching system for determination of objects positions it was proposed to receive data from several sources and send them to the user by means of GSM modules and short messages of the SMS. Formats of messages are shown on fig.2.

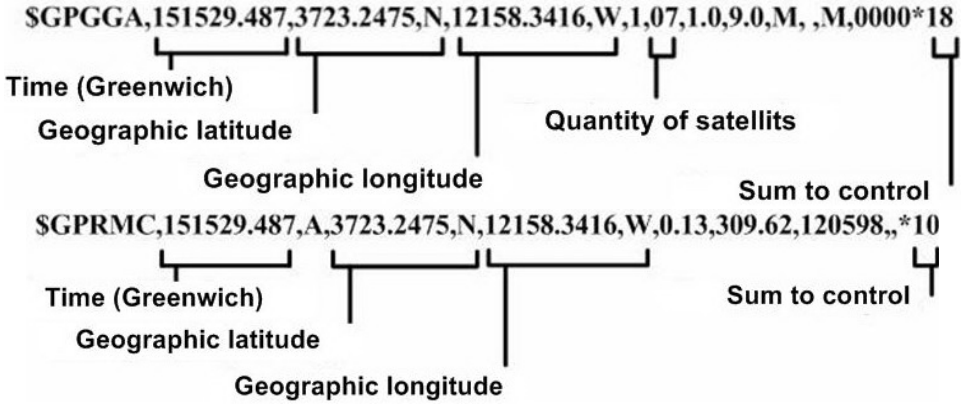

Fig.2. Formats of messages

To do this it is necessary to perform sending through port in the GSM module specially created line; receive acknowledgment reception (symbol «>»); then perform the sending of text messages (up to 140 symbols in the Latin alphabet); and, in case of successful receiving, accept from GSM answer «OK».

To implement of these functions the data transfering system (fig.3) constructs of two serial input-output ports to exchange data with GPS and GSM modules and processor. For programming and simulation of the main blocks of the transfering system the following software are used: Xilinx ISE Design Suite; Aldec Active HDL; Quartus II Web Edition. The project contains nine files with the description of devices and one library for used data types and constants.

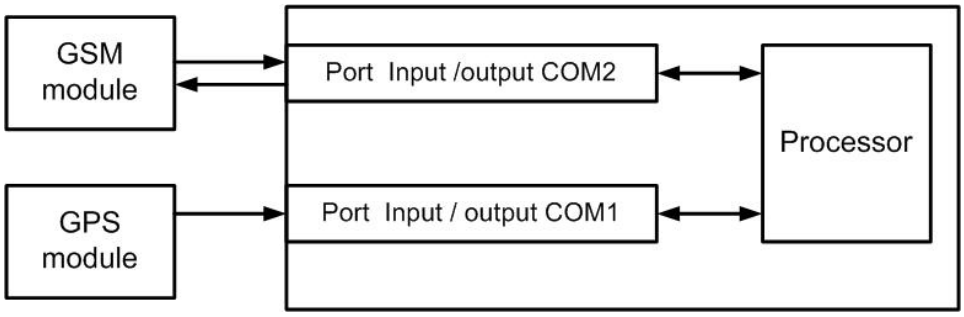

Fig.3. Structure of data transfering system

For the project, based on chip of XC3S500E, it is enough to use 8 bit ALU, 256 bytes of data memory, 256 words of commands memory and 16 bit data buffer for ports of input-output FIFO. To develop and test the board Spartan-3E Starter Kit (Xilinx. [3]) and software Xilinx ISE Design suite are used (fig.4).

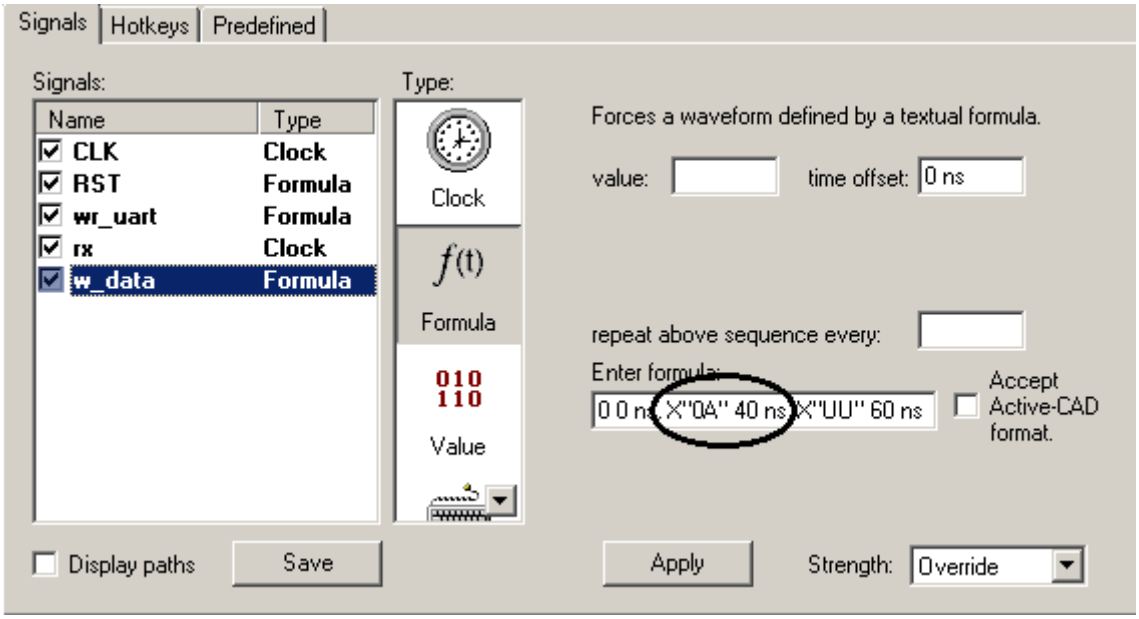

Fig.4. Demonstration of Xilinx ISE Design suite using

Figure 5 shows the time diagram of the output port, test frequency is accepted 50 MHz. The next lines are shown: CLK - input clock signal (50 MHz); RST - reset signal; w_data - output byte; tick - resample the signal from the baud rate generator; tx - output port line; array_reg - an array of data FIFO buffer. Thus on the first clock period with the high front of a signal (from 20 ns to 40 ns) performed reset for resetting to zero all registers and establishment of the initial values. Then (in an interval of 40 – 60 ns) in the output register are written 0A value (in binary - 00001010).

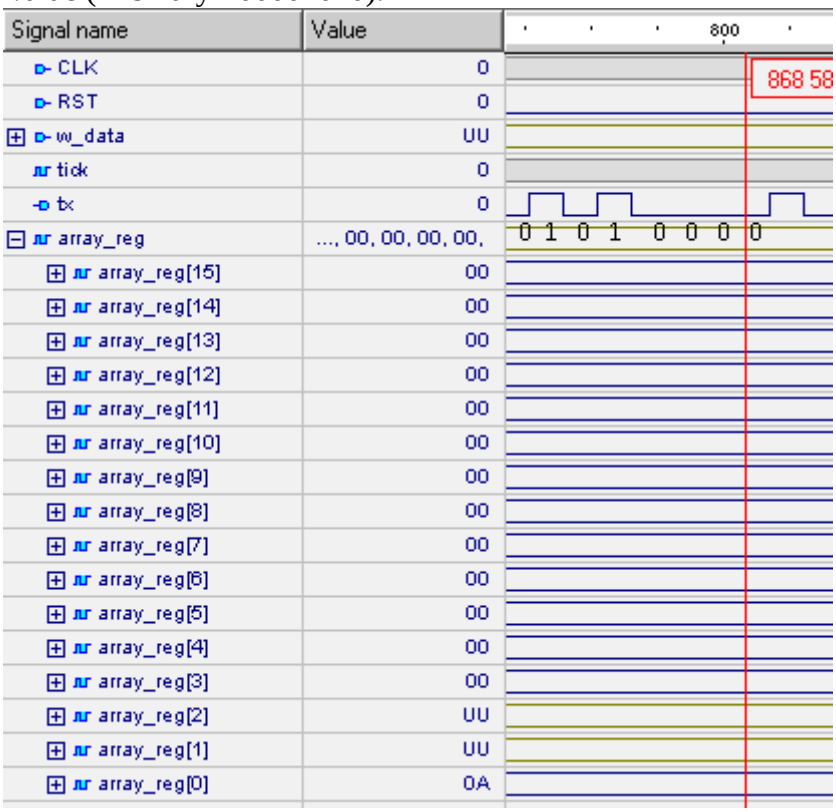

Fig.4. Time diagram for data transmission port

It is necessary to note, that transmission of binary data performed sequentially, therefore reading output byte is performed in the opposite direction. To receive data on input line **rx** a periodic signal with a frequency of 9600 Hz is generated. The simulation result is shown on Fig. 5 (rx- input data line; r_data-byte received; array_reg - buffer FIFO).

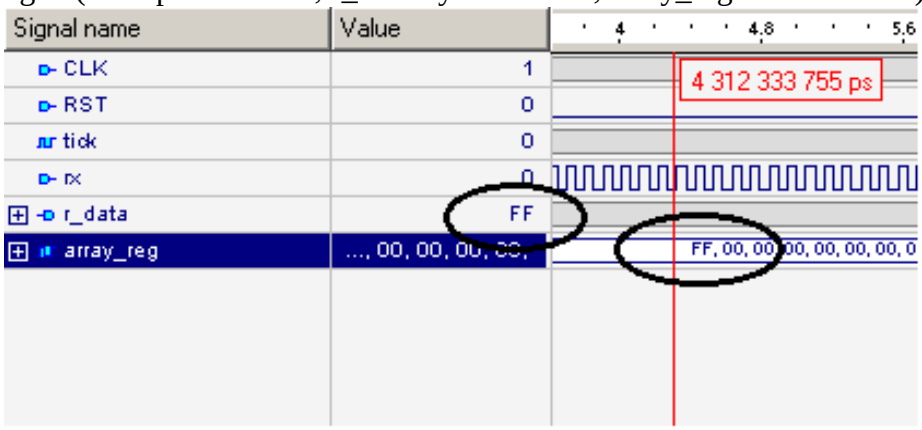

Fig.5. The time diagram of the data receiving port

Also the special processor is developed. It performs the basic arithmetic operations (addition, subtraction, increment), as well as the bit-wise logical operations to verify the data correctness. Processor uses two types of memory: code memory to store instructions and data memory. Fig.6. demonstrates a program fragment.

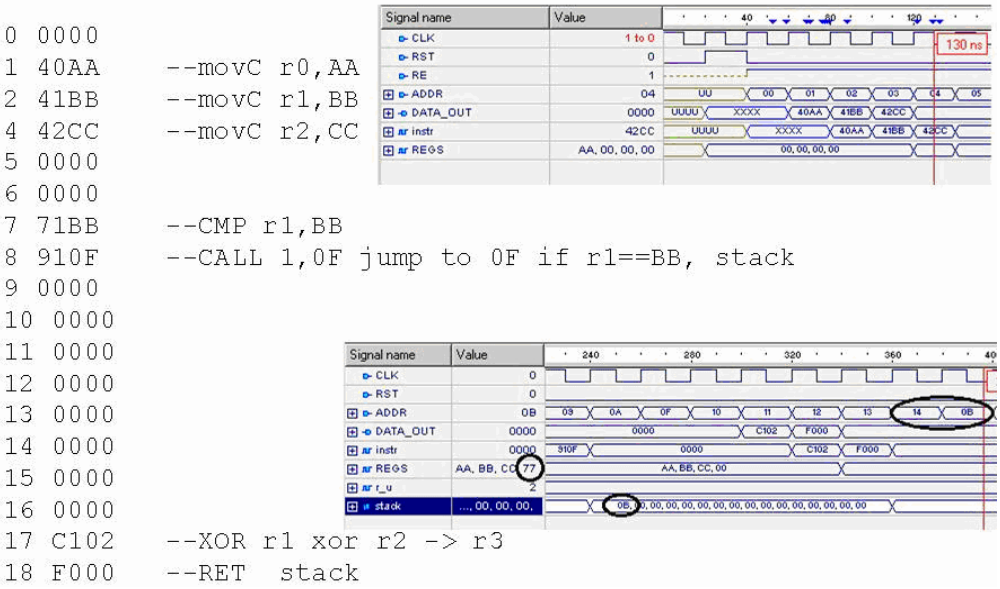

Fig.6. Demonstration of a program fragment.

Simulation using Xilinx ISE Design suite allows to develop effective data transfering system.

Conclusion

This paper demonstrates the results of designing and simulation of the data transfering system. The developed controller can be used as basic for development of industrial devices of specialized assignment; the received results also can be used as a bright example for the students training.

References:

B. Brodersen. Wireless Sytem-on-a-Chip Design. – http://bwrc.eesc.berkelay.edu
http://vistgroup.ru., http://xilinx.com