PERFORMANCE ANALYSES OF SPECULATIVE VIRTUAL CHANNEL ROUTER FOR NETWORK-ON-CHIP

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Abstract

Network -On-Chip (NoC) is becoming the backbone of System on chip (SoC) architecture and router is the heart of an NOC architecture. This paper explores two types of Routers. First is the Speculative Virtual Channel Router for Network-On-Chip (NoC) and second, non- speculative Virtual Channel Router for Network-On-Chip (NoC). In the speculative Virtual channel router, Speculative virtual channel allocation and the speculative switch allocation takes place at the same time on the other hand in non-speculative virtual channel route channel allocation and switch allocation takes place serially. Major components of proposed routers are Input Port, Allocators and the contention free crossbar switch. Performance analysis on two parameters, Area and Delay for both types of design is presented with the help of "Xilinx ISE-13.1" design suite.

Keywords: Speculative, contention free cross bar, router, virtual channel

Introduction

System-on-Chip (SoC) design methodologies provide a powerful, capable and flexible solution to integrate complex systems on a single chip with the development of high-density VLSI technology. As the semiconductor technology increases we can place more number of heterogeneous IP (intellectual property) cores such as processors, DSPs, memory blocks, dedicated hardware accelerators, etc... on a single chip but these System-on-Chip(SoC) are major challenges in parameters like Delay, area, high-performance etc…[1] Recently Network-on-Chip is developed for better communication in System of chip; Network-on-chip does not uses dedicated wires for communicating between PE (Processing Element) instead it use exchange messages between PE (Processing element) over the network. [2]

Some of reason for which SoC need (Network-on-Chip) NoC are; by using NoC technology we can reduce the wire length required to route the data in SoC, also the longer wires have high electrical capacitance which lead to power dissipation, NoC technology simplifies the hardware requirement for routing and switching function. There are several architectures that can be used for Network-on-chip. However NoC's have three basic building blocks namely Network interface, switch and link [3]. Function of network interface is to connect the IP blocks to the network, it also convert request in to packet and further packet is divided into flits (Flow control unit), function of switch or router is to dispatch the packet in the network depending on routing scheme used and Link is used to connect the IP block to switch or switch to switch.

Outline for this paper is as follows: After the introduction, we discussed the concept of speculation in section 2. Then we discuss the concept of contention free crossbar in section 3.In section 4 we talk about the speculative virtual channel router without contention free

crossbar and non-speculative virtual channel router with contention free crossbar. In sections 5 and 6 we made comments on results.

Speculation

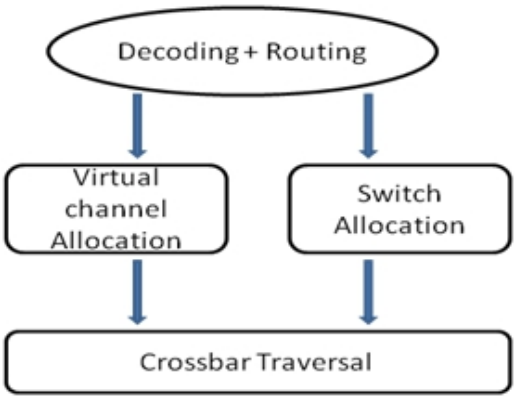

Fig1. Flow chart of packet in speculation

Basic concept of speculation is that, the Virtual channel allocation takes place in parallel with the Switch allocation as shown in fig above. Speculation can be understood by considering an example bellow.

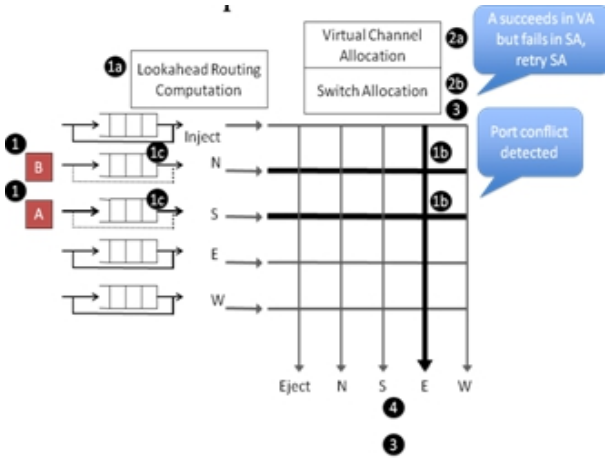

Fig2. Block diagram for speculation concept

In fig above we have five buffered input port out of five ports, two input buffered port wish to transfer the data. Let us consider two data packet be “A” and “B”. Initially destination of both the packet is checked and it was found that both wish to acquire the “E” output port of crossbar. In the first attempt one out of two packet which has higher priority has been allocated the virtual channel and at the same time switch allocation is done for the same packet due to this one packet is routed to the “E” output port of the crossbar at a single clock, let us consider this packet be “B”. Since both “A” and “B” wish to acquire same output port therefore along with packet “B”, Packet “A” succeeds in virtual channel allocation but fails in switch allocation, this packet will retry for the switch allocation in next clock after the transfer of “B” packet. Speculation reduces the delay since it perform both the channel allocation and switch allocation in single clock and if packet fails in switch allocation, that packet is transfer in next clock till that time it is stored in buffers available at input port and packet does not get lost, this idea is known as speculation.

Contention Free Crossbar

Crossbar switch is the heart of data routing, purpose of crossbar switch is to route data from one input port to any of output port. An arbiter is the important component of crossbar switch. Arbiter is nothing but the device which selects one output from the number of input

depending upon the logic we apply. In case of crossbar, we are having an arbiter which is having the same number of input and output that of crossbar. At the input of crossbar we have to identify three quantities i.e. Data, destination and request. Data is the information that we wish to route at the output side, destination is the address of the output port at which we want to send the data and third quantity is nothing but the request, when it is high it means that data of that respective input port is to be routed. Each input port of crossbar is associated with individual arbiter i.e. if we have 5*5 crossbars then at every input port we have one arbiter which itself has 5 input and 5 output, these five inputs of arbiter are nothing but the request from each input port of crossbar and output of arbiter is the grants which is connected to the output port of crossbar. Bellow FSM decides the high and low condition for the grant, depending on these condition packets from input side is routed to the output side of the crossbar.

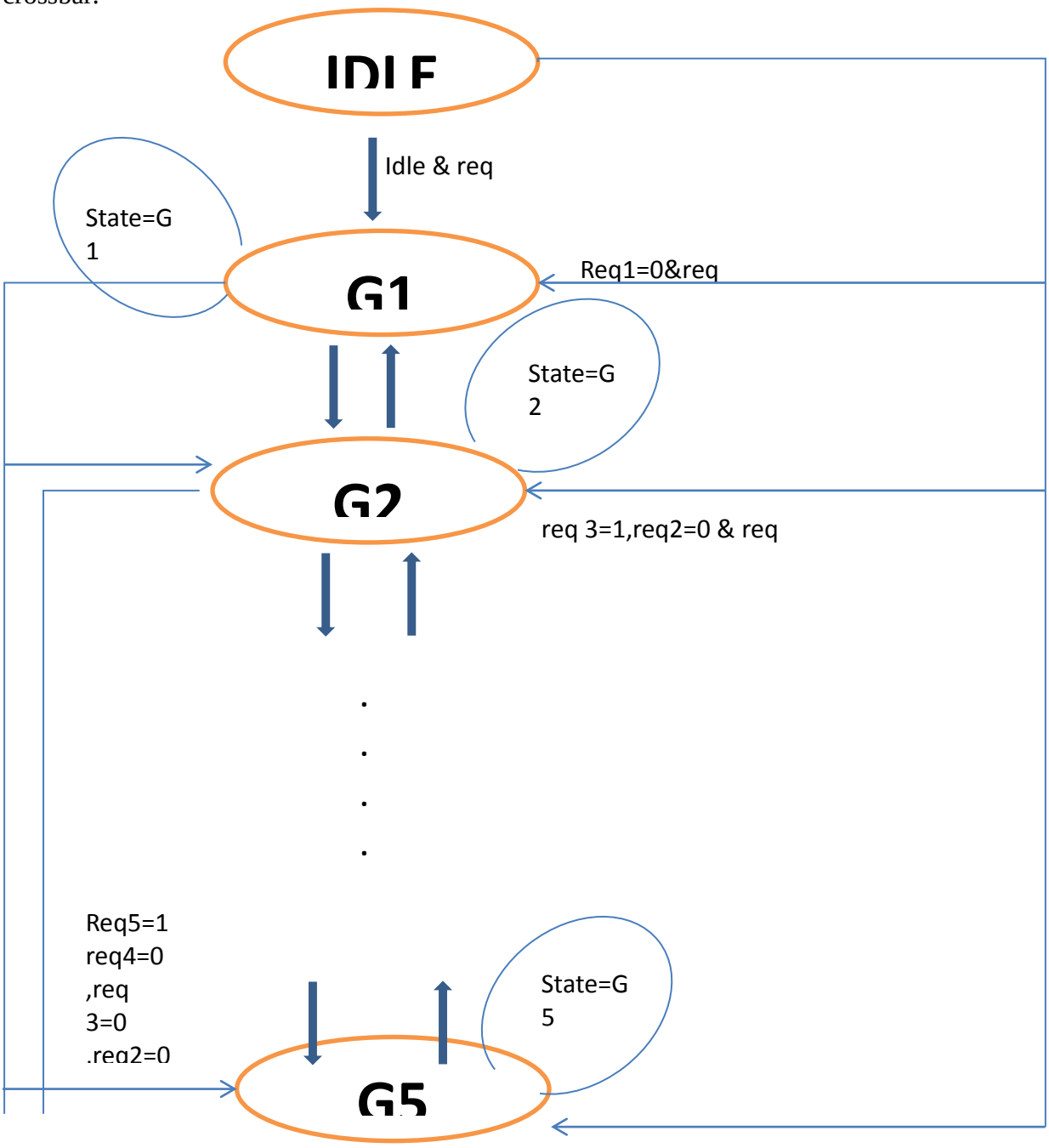

Fig3. FSM table for arbiter.

In crossbar switch which are having arbiter as it component it might be possible that if two or more packets at the input of crossbar send request to acquire same output port than it might be possible that some packets get lost because only one packet at a time can access the crossbar switch. In order to avoid this problem we use buffers/memory along with arbiter so that packet which are failed to acquire output port of crossbar can be stored in that buffer and can be transferred in next clock cycle, this type of crossbar is nothing but the contention free crossbar. The block diagram for Contention free crossbar is shown bellow.

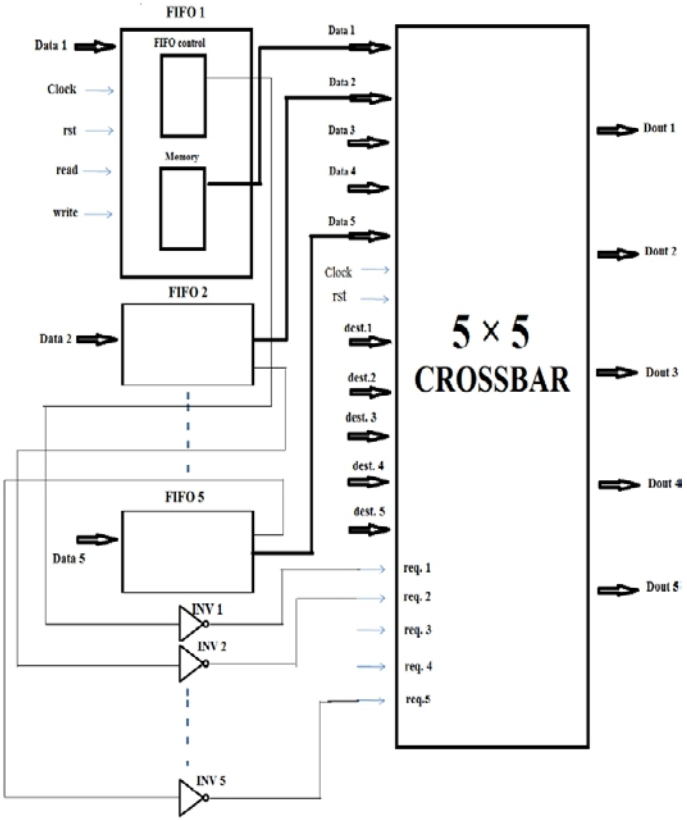

Fig4. Block diagram Contention free crossbar

In contention Free crossbar switch we have used an FIFO unit that will store the data from one user and data from other user will be routed successfully when two different users are requesting the same output port. FIFO unit consist of FIFO control unit and memory unit. FIFO control unit have clock, reset, write request & read request as input and address, empty, full, read enable, write enable as output. Whenever any user send data the request of FIFO control unit is made high and write enable signal goes high and the data is stored in memory unit. As the memory is not empty therefore request of crossbar goes high and data is routed successfully. In our contention free crossbar switch all the data is routed via memory unit, hence when two user request for the same output port at same time than one data is transferred and other is stored in memory unit for the time first data routed successfully, in next clock value of empty signal is checked again this time empty signal is low and again the request is made to send the second data. [4][5][6][7]

Speculative virtual channel router without contention free crossbar and non-speculative virtual channel router with contention free crossbar.

The basic difference between speculative virtual channel router and non-speculative virtual channel router is that in speculative virtual channel router virtual channel allocation takes place in parallel to the switch allocation; on the other hand in non-speculative virtual channel router first the channel allocation takes place and then the switch allocation. In this

paper we had compared the speculative virtual channel router without contention free crossbar (simple crossbar) Vs non-speculative virtual channel router with contention free crossbar. Reason for comparing this specific configuration is, in first configuration we are using speculation technique along with the simple crossbar switch, here the speculation technique allocate the virtual channel at the input port and switch at the crossbar so that the packet is directly transferred to output. In second configuration we are using the buffers at the input of crossbar so that if the user has higher frequency to transfer packet then the packet does not lost instead stored in the memory unit and transferred in next clock.[8]

Result

All the parameter analysis regarding to the above work is done for Spartan 3 (XC3S50) device and "Xilinx ISE-13.1" whose results are shown bellow.

The area analysis for Speculative virtual channel router without contention free crossbar (simple crossbar) is shown below.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	540	1,536	35%
Number of 4 input LUTs	293	1,536	19%
Number of occupied Slices	343	768	44%
Number of Slices containing only related logic	343	343	100%
Number of Slices containing unrelated logic	0	343	0%
Total Number of 4 input LUTs	293	1,536	19%
Number used as logic	285		
Number used as Shift registers	8		
Number of bonded IOBs	86	124	69%
Number of BUFGMUXs	1	8	12%
Average Fanout of Non-Clock Nets	2.94		

Table1. Area analysis for speculative virtual channel router

The area analysis for Non-Speculative virtual channel router with contention free crossbar is shown bellow.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	561	1,536	36%
Number of 4 input LUTs	882	1,536	57%
Number of occupied Slices	527	768	68%
Number of Slices containing only related logic	527	527	100%
Number of Slices containing unrelated logic	0	527	0%
Total Number of 4 input LUTs	882	1,536	57%
Number used as logic	746		
Number used as Shift registers	136		
Number of bonded IOBs	86	124	69%
Number of BUFGMUXs	1	8	12%
Average Fanout of Non-Clock Nets	3.33		

Table2. Area analysis for non- speculative virtual channel router

Conclussion

From last section we conclude that area required for speculative virtual channel router without contention free crossbar is 343 slices i.e. 44% of total slices available, where as in case of non-speculative virtual channel with contention free crossbar the area required is 527 slices which is 68% of available slices. Therefore area required for speculative virtual channel router is greater than that of non-speculative virtual channel router. Other than the area, frequency is also an important factor. The minimum period for speculative virtual channel router without contention free crossbar (Simple crossbar) is 3.800 ns therefore speculative virtual channel router work on maximum of 263.130 Mhz. On other hand non-speculative virtual channel router with contention free crossbar the minimum period is 8.247 ns so it can work on maximum frequency of 121.254 Mhz.

Configuration	**Area**	**Maximum frequency**
Speculative virtual channel router without contention free crossbar	44%	263.130 MHz
Non-Speculative virtual channel router with contention free crossbar	68%	121.254 MHz

Table3. Comparative table on the basis of analysis done for Spartan 3 (XC3S50) device and "Xilinx ISE-13.1"

References:

Son Truong Nguyen and Shigeru Oyanagi "The Design of On-the-fly Virtual Channel Allocation for Low Cost High Performance On-Chip Routers" *First International Conference on Networking and Computing 2010 IEEE*

Mohamed horchani, Mohamed ATRI and Rached TOURKI "Design of a NoC-router guaranteeing QoS based on VirtualChannels reservation" *International Conference on Signals, Circuits and Systems 2008 IEEE*

David Atienzaa, Federico Angiolini, Srinivasan Muralia, Antonio Pullinid, Luca Beninic and Giovanni De Micheli "Network-on-Chip design and synthesis outlook" *INTEGRATION, the VLSI journal 41 (2008) 340–359 Science Direc*t

George F. Georgakopoulos "Buffered Cross-Bar Switches, Revisited: Design Steps, Proofs and Simulations Towards Optimal Rate and Minimum Buffer Memory" *IEEE/ACM transactions on networking, vol. 16, no. 6, december 2008.*

Guannan Qu, Hyung Jae Chang, Jianping Wang, Zhiyi Fang and S. Q. Zheng "Contention-Tolerant Crossbar Packet Switches without and with Speedup" *IEEE ICC 2010.*

Mohammad Ayoub Khan and Abdul Quaiyum Ansari "modelling and simulation of 128-bit crossbar switch for network –onchip" *International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.3, September 2011.*

Lotfi Mhamdi and Kees Goossens "Buffered Crossbar Fabrics Based on Networks on Chip" *8th Annual Communication Networks and Services Research Conference 2010 IEEE.*

Arnab Banerjee, Pascal T. Wolkotte, Robert D. Mullins , Simon W. Moore and Gerard J. M. Smit "An Energy and Performance Exploration of Network-on-Chip Architectures" *IEEE transactions on very large scale integration (vlsi) systems, vol. 17, no. 3, march 2009.*