# A NOVEL PRESENTATION OF PERES GATE (PG) IN QUANTUM-DOT CELLULAR AUTOMATA(QCA)

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**Abstract**

QCA technology is a possible substitution for semiconductor-based technology. This paper presents a novel design of a Quantum-dot Cellular Automata (QCA) Peres Gate (PG) and its simulation. Peres Gate (PG) is a reversible logic gates. Reversible logic gates are attracting a lot of attention due to their zero power dissipation under ideal conditions. Reversible logic circuits are useful for constructing quantum computers.

**Keywords:** QCA, Peres Gate (PG), QCA Designer, Majority Voter Gate

## Introduction

Day by day aggressive scaling down of CMOS devices results in several physical limits such as high leakage current, high power density levels, high lithography cost, and limitation of speed in GHz range. It is predicted that these limitations foreshadow the eventual end of scaling trend of traditional CMOS technology. Quantum-dot Cellular Automata (QCA) is one possible and promising alternative of CMOS technology and it provides a revolutionary approach to computing at nano-scale (Lent et al. 1993). It offers a new method of computation and information transformation (Orlov, A. O, 1997), in which rather than using voltages on transistors to encode information, QCA exploits interacting electric or magnetic field polarization. QCA is a novel and potentially attractive nano-technology due to its extremely small feature sizes, faster speed, higher scale integration, higher switching frequency, and ultra low power consumption (Lent, C. S., 1997) than transistor based technology.

**The Basics Of QCA**

QCA make use of arrays of coupled quantum dots to encode and process binary information. A four-dot quantum cell consists of four dots positioned at the corners of a square with two extra mobile electrons as shown in Fig.1 (a). Another type of QCA cell shown in Fig.1 (b) also consists of four dots at the middle of the sides of cells. Electrons can tunnel from dot to dot within a cell, but unable to travel beyond the cell boundaries to neighboring cells. Coulomb repulsion between the electrons will force them to occupy diagonally opposite dots. There are two equivalent energetically minimal arrangements for the electrons in a QCA cell (Meurer, B., 1993; Lent 1997)., i.e. the polarization P = +1 (representing logic 1) and P = –1 (representing logic 0) shown in Fig.1(c).

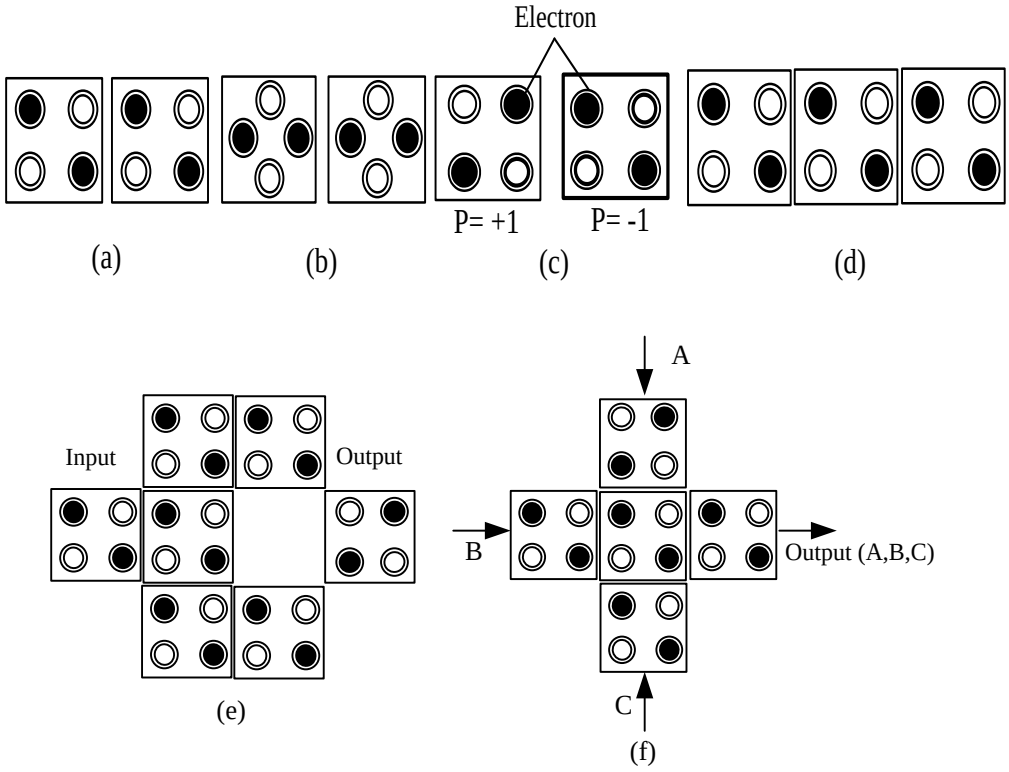


Figure 1: (a) QCA Cells with 90-degree orientation (b) QCA Cells with 45-degree orientation (c) Logical representations of QCA cells (d) Normal QCA wire (e) QCA inverter (f) QCA majority gate

The QCA wire is a horizontal row of QCA cells and a binary signal propagates from left-to-right due to electrostatic interactions between adjacent cells. The normal QCA wire is shown in Fig.1 (d). In QCA Inverter Gate is the basic QCA logic element. In this gate signal comes in from the left, splits into two parallel wires, and is inverted at the point of convergence

as shown in Fig.1 (e). The polarization of the output QCA cell is the opposite of the polarization of input QCA cell. One of the basic QCA fundamental elements is QCA Majority Voter (MV) gate as shown in fig.1(f), which is a 3-input majority gate and composed of five cells. Three of these, representing the inputs cell, are labeled A, B, and C and the center cell is the device cell that performs the calculation (Ma, X., 2008). The remaining cell, labeled OUT (A, B, C), provides the output. This gate performs the Boolean function, OUT(A, B, C) = Maj(A, B, C) = AB+BC+CA. Outputs "1" if there are two or more 1s in an input pattern, otherwise the output is "0".

**QCA XOR Gate**

In addition to AND, OR, NOT, NAND and NOR gates, exclusive-OR (XOR) and exclusive-NOR (XNOR) gates are also used in the design of digital circuits. These have special functions and applications. These gates are particularly useful in arithmetic operations as well as error-detection and correction circuits. XOR and XNOR gates are usually found as 2-input gates. No multiple-input XOR/XNOR gates are available since they are complex to fabricate with hardware. The exclusive-OR (XOR) performs the following logic operation: A⊕B = A'B+ AB'. The QCA implementation for XOR gate is shown in Figure 2.

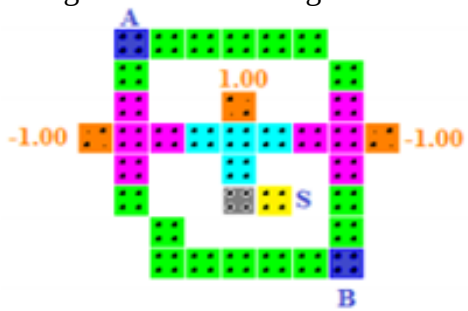


Figure 2: A QCA XOR gate

**Peres Gate (PG)**

Peres Gate (PG) is composed of two XOR gate shown in Figure 2 and one AND gate. Figure 3 shows a 3x3 Peres gate (Peres, A., 1985, Ali M., 2012). The input vector is I (A, B, C) and the output vector is O (P, Q and R). The output is defined by P = A, Q = A⊕B and R=AB⊕C. Quantum cost of a Peres gate is 4.

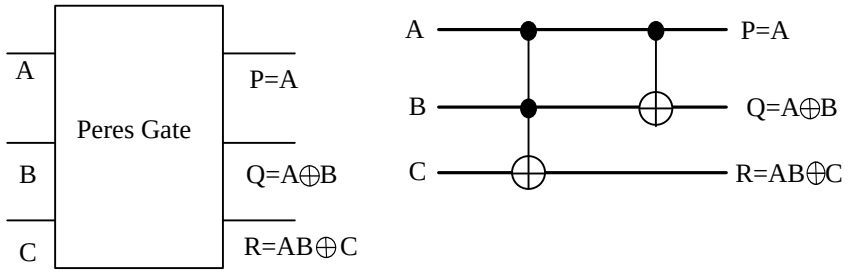


Figure 3: Peres Gate

**Table 1:** Truth Table of Peres Gate

| Input | | | Output | | |
|---|---|---|---|---|---|
| A | B | C | P | Q | R |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

## Peres Gate (PG) in QCA

The block diagram of Peres Gate in QCA is shown in Figure 4. The QCA layout structure of the Peres Gate is shown in Figure 5 that is composed of 96 cells. Three of these, representing the inputs to the cell, are labeled A, B and C. Using the terminology of (Ma, X., 2008, Peres, A., 1985) the center cell is the "device cell" that performs the calculation. The remaining cell, labeled P, Q, and R provide outputs. The circuit shown in Figure 5 performs the Boolean functions P = A, Q = A⊕B and R = AB⊕C.

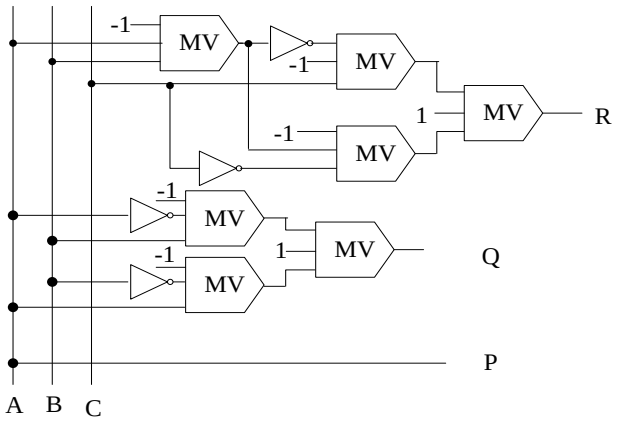


Figure 4: Block Diagram of the Peres Gate in QCA

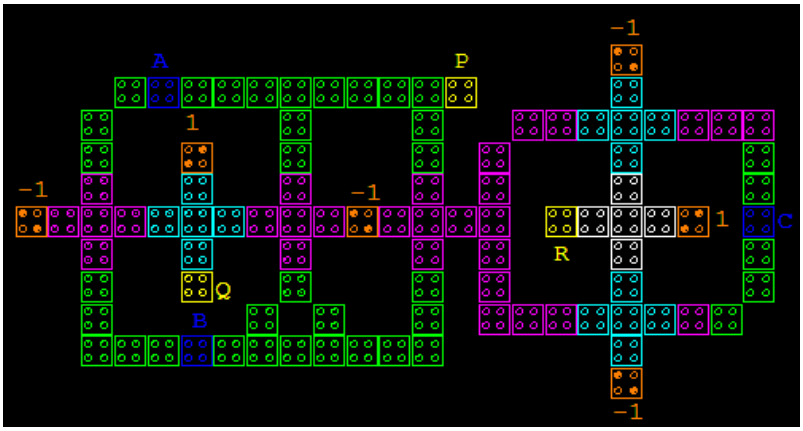


Figure 5: QCA layout structure of the Peres Gate

## Simulation Results

The Peres Gate layout has been simulated using QCA Designer version2.0.3; a layout and simulation tool for QCA. The simulation result for a Peres Gate is shown in Figure 6. In this Simulation we have used the coherence vector computational engine and the following parameters: (18 nm × 18 nm) cell size, 11.5 nm cell-to-cell distances, and 5 nm dot size and 65 nm radius of influence.

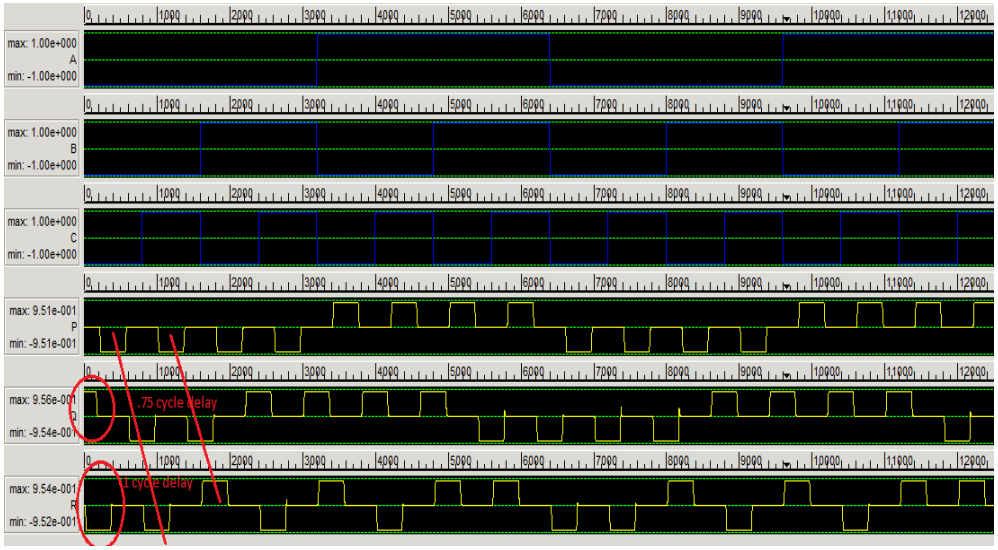


Figure 6: Simulated waveforms for Peres Gate

**Table 2:** Result analysis of proposed Peres Gate in QCA

| Parameter | Value |
|---|---|
| Number of cells | 99 |
| Covered area ($\mu m^2$) | 0.1008 |
| Clock used | 4 |
| Time delay (clock cycle) | 1 |

## Conclusion

In this paper, a novel Peres gate has been proposed. This gate has been implemented in one layer and using only 99 QCA cells. As far as verifying the functionality, this proposed gate has been proven by some physical relations as well as computer simulations. These designs have been verified in QCADesigner, a QCA simulation and layout verification tool. This design is very useful for future ultra-low power digital circuits and quantum computers.

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