FPGA BASED DESIGN OF 1D DCT/IDCT FOR MIMO OFDM CHANNEL ESTIMATION

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Abstract

Orthogonal frequency division multiplexing (OFDM) is a popular digital modulation scheme for high data rate wireless transmission. A multi input multi output (MIMO) configuration is the combination of multiple antennas at the transmitter and receiver enhances the operation of OFDM. In this paper, a study of channel estimator for less complexity and good channel tracking ability for MIMO-OFDM wireless transmission is carried out. An estimator with combination of Least Square Error (LSE) estimator with Discrete Cosine Transform (DCT) is designed as the channel estimator for MIMO-OFDM system for wireless transmission. The designing is simulated and validated using ModelSim which is a functional hardware simulation, and the Verilog source code is synthesized for Vertex 5 Field Programmable Gate Array (FPGA) component. It is observed that the LSE reduces the complexity, whereas DCT increases the efficiency of the transmission.

Keywords: Orthogonal frequency division multiplexing, Least Square Error, Discrete Cosine Transform, channel estimation

Introduction

Wireless Systems operate in an environment which has some specific properties compared to fixed wire line systems and this requires special

design considerations. In a wired network, there are no fast movements of terminals or reflection points and the channel parameters change very slowly. The time dispersion is less severe in a wired system, though it might still be a hard problem due to high data rates. Due to the changes of the terminals in mobile communication system, the received signal strength as well as the phase of the received signal change rapidly. The signal transmitted over the radio channel is reflected by buildings and other means of transportation on the ground, leading to different paths to the receiver. Hence if the length of the paths differs, the received signal will contain several delayed versions of the transmitted signal according to the channel impulse response.

For the transmission of data such as video, high quality audio and mobile integrated service, the digital networks require high bit rates. High bit rate transmission of data over mobile radio channels, causes channel impulse response to extend over many symbolic periods which lead to Inter Symbol Interference (ISI). In wireless communication systems, Orthogonal Frequency Division Multiplexing (OFDM) is commonly used for the data transmission. OFDM has the capability to transmit high data rate signals with large bandwidth efficiency and avoids multi path delay (Coleri, 2002). The performance of the communication system requires accurate channel estimation, as OFDM uses the coherent receivers. There are mainly two methods of channel estimation in OFDM, they are pilot aided channel estimation and blind channel estimation. Due to complexity and slow convergence, blind channel estimation is not commonly used in channel estimation process, whereas the pilot aided channel estimation gives high accuracy and it has high processing speed, and thus it is commonly used in channel estimation (Wang, 2012). In order to achieve high data rate transmission, multiple input multiple output (MIMO) communication systems are implemented with OFDM technique over broad band wireless channels. The capacity of the system and diversified gain can be improved by MIMO systems. Hence the new generation wireless transmission uses the combination of MIMO and OFDM technologies (Diallo, 2009). In MIMO-OFDM systems, the channel state information (CSI) is usually required at the receiver side and thus sub channels between each antenna link have to be individually estimated. Dynamic channel estimation is necessary as radio channel are frequency selective and time-dependent. Channel estimation based on pilots with transform domain noise reduction is known as smoothing which is implemented in coherent MIMO-OFDM receiver. In order to significantly reduce the noise on the estimated channel coefficients, the Discrete Fourier Transform method is employed. However, “border effect” may occur when the number of Inverse Fast Fourier Transform points is different from the number of modulated subcarriers. This may be a real problem because the vast majority of modern multicarrier systems contain

null carriers at the spectrum extremities. DCT can be instead of DFT for mitigating the impact of the ”border effect” owing to its capacity to reduce the high frequency components in the transform domain at the price of a weaker noise reduction (Kobayashi, 2004). Nevertheless, the complexity and latency of the classical DCT may cause problems, especially in MIMO-OFDM systems where all the subchannels between the antenna links have to be individually estimated. To reduce the complexity implementation, the present study proposed to divide the whole DCT window into small overlapping blocks and reported the use of Modified DC algorithm to further reduce the channel estimation complexity. In addition, the present study also reported a hardware implementation of the proposed channel estimation design for Vertex 5 FPGA component.

Mimo - OFDM model

Selection of carrier spacing, so that the subcarrier is orthogonal to the other subcarriers in multicarrier modulation is defined as OFDM. The two signals are orthogonal if their dot product is zero. Large number of closely spaced orthogonal subcarriers, transmitted in parallel is used in OFDM. These subcarriers are modulated with the conventional modulation method such as Quadrature Phase Shift Keying, Quadrature Amplitude Modulation etc. (Kobayashi, 2004). The Figure 1(a) shows the spectrum of orthogonal carrier signal and Figure 1(b) shows the time domain representation of orthogonal carrier.

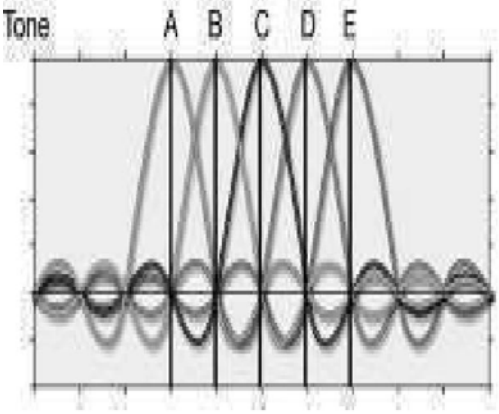

Figure1(a): Spectrum of Orthogonal carriers representation

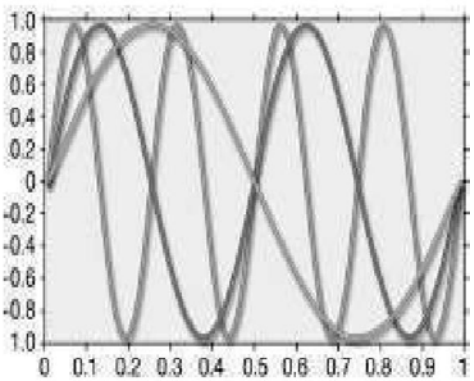

Figure1(b): Time domain of Orthogonal carriers

As the subcarriers are orthogonal to each other the spectrum there is no interference between the carrier, allowing them to be as close as possible.

Mathematically, we consider the signal ψ then,

$$\int_0^T \varphi_p(t)\varphi_q^*(t) = k \; for \; p = q$$
$$= 0 \; for \; p \neq q \qquad 1$$

Where $\varphi_p \; and \; \varphi_q$ are pth and qth element in the set. The signals are orthogonal if the integral value is zero and T is a time period of the signals.

To generate a baseband OFDM symbol, a serial digitized data stream is first modulated using common modulation schemes such as the phase shift keying (PSK) or quadrature amplitude modulation (QAM). These data symbols are then converted to parallel streams before modulating subcarriers. Subcarriers are sampled with sampling rate N /T, where N is the number of subcarriers and T is the OFDM symbol duration. The frequency separation between two adjacent subcarriers will be 2π / N, and the samples on each subcarrier are summed together to form an OFDM sample. An OFDM symbol generated by an N-subcarrier OFDM system consists of N samples and the m-th sample of an OFDM symbol is given by

$$X_m = \sum_{n=1}^{N} e^{j2\pi mn/N} \quad 0 \leq m \leq N-1 \qquad 2$$

where X_n is the transmitted data symbol on the nth carrier. Equation 2 is equivalent to the N-point inverse discrete Fourier transform (IDFT) operation on the data sequence with the omission of a scaling factor. It is well known that IDFT can be implemented efficiently using inverse fast Fourier transform (IFFT). Therefore, in practice, the IFFT is performed on the data sequence at an OFDM transmitter for baseband modulation and the FFT is performed at an OFDM receiver for baseband demodulation. The sub-channel bandwidth is given by

$$f_{samp} = \frac{1}{T} = \frac{t_{samp}}{N} \qquad 3$$

where f_{samp} is the sample rate ,and T_s is the symbol time. Finally, a baseband OFDM symbol is modulated by a carrier to become a band pass signal and transmitted to the receiver. In the frequency domain, this corresponds to translate all the subcarriers from baseband to the carrier frequency simultaneously (Diallo, 2010).

The block diagram of MIMO-OFDM is as shown in Figure 2. The binary information is first grouped and mapped ac-cording to the modulation in “signal mapper” (Colieri, 2002). After inserting pilots either to all sub-carriers with a specific period or uniformly between the information data sequence, IDCT block is used to transform the data sequence of length into time domain signal with the following equation,

$$x(n) = IFFT\{X(K) = \sum_{K=0}^{n-1} X(K) e^{j2\pi kn/N} \qquad 4$$

For n = 0, 1…..n-1, where N is the number of FFT points and k the subcarrier index.

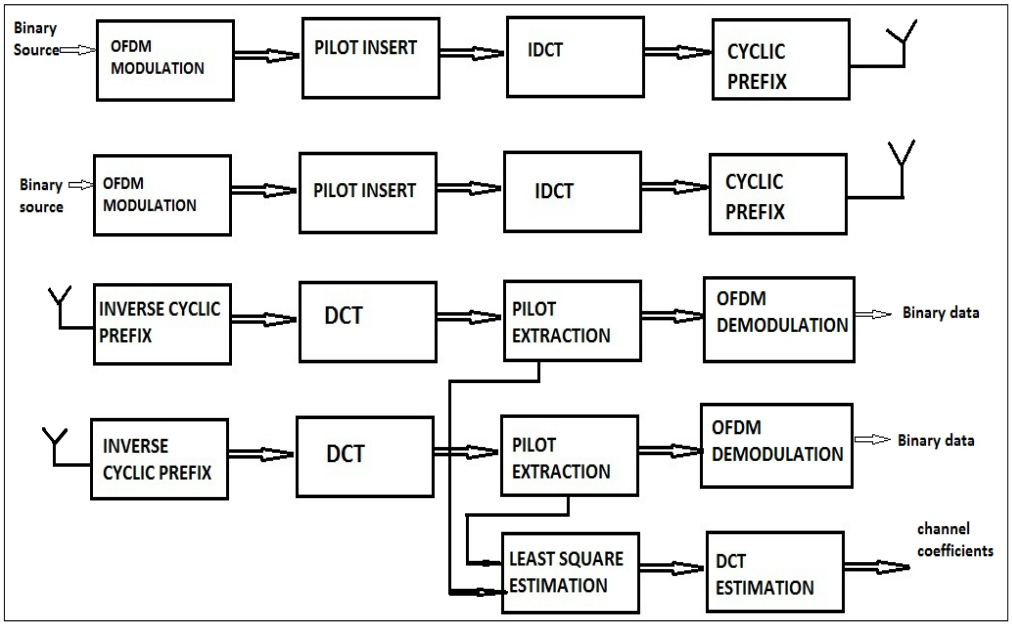

Figure 2. Block Diagram of MIMO-OFDM

After IDCT block, guard time is chosen to be larger than the expected delay spread, is inserted to prevent inter-symbol interference. This guard time includes the cyclically extended part of OFDM symbol in order to eliminate inter-carrier interference (ICI). The use of the cyclic prefix (CP) allows both the preservation of the orthogonality between the tones and the elimination of ISI (inter symbol interference) between consecutive OFDM symbols (Chen, 2006). The transmitted signal x(n) will pass through the frequency selective channel with additive noise. The received signal is given by the following equation,

$$y(n) = x(n) \otimes h(n) + w(n) \qquad 5$$

where w (n) is Additive White Gaussian Noise (AWGN) and h (n) is the channel response.

Modified Discrete Cosine Transform

The modified discrete cosine transform (MDCT) is a lapped transform based on the discrete cosine transform, with the additional property of being lapped. It is designed to be performed on consecutive blocks of a larger dataset, where subsequent blocks are overlapped so that the last half of one block coincides with the first half of the next block. This overlapping, in addition to the energy-compaction qualities of the DCT, makes the MDCT especially attractive for signal compression applications,

since it helps to avoid artifacts stemming from the block boundaries. As a result of these advantages, the MDCT is employed in most modern lossy audio formats (Princen 1987).

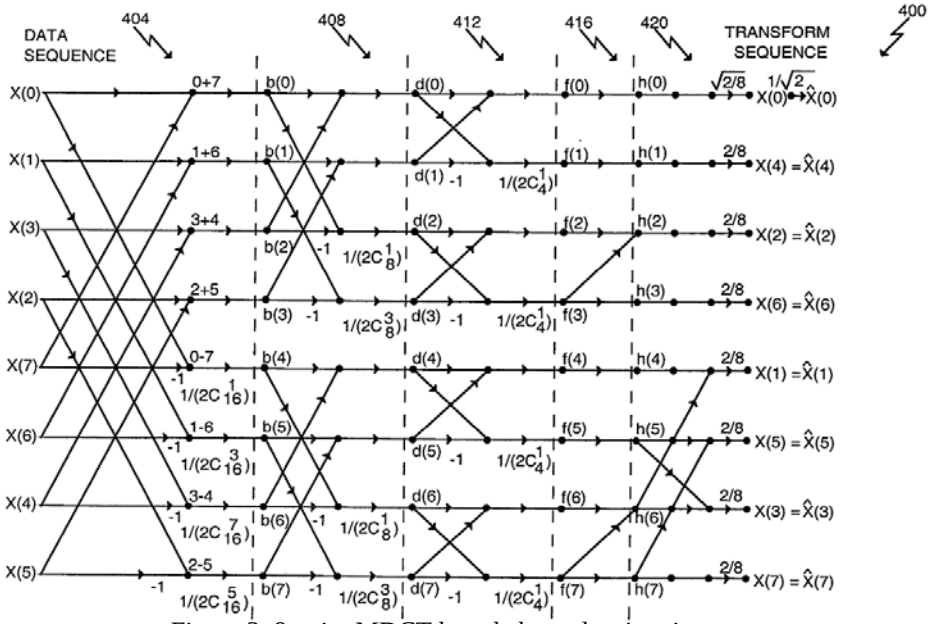

Figure 3. 8 point MDCT based channel estimation

As a lapped transform, the MDCT is a bit unusual compared to other Fourier-related transforms as it has half as many outputs as inputs (instead of the same number). It is a linear function $F: \mathbf{R}^{2N} \rightarrow \mathbf{R}^{N}$ (where **R** denotes the set of real numbers). The 2*N* real numbers x_0, x_{2N-1} are transformed into the *N* real numbers X_0, X_{N-1} given as

$$X(K) = \sum_{N=0}^{n-1} x(n) \cos\left[\frac{\pi}{2N}\left(2n + 1 + \frac{N}{2}\right)(2K + 1)\right] \qquad 6$$

where K=0, 1..... (N/2)-1.

As there are different numbers of inputs and outputs, it may look that the MDCT should not be invertible. However, perfect invertibility is achieved by adding the overlapped inverse MDCTs of subsequent overlapping blocks, causing the errors to *cancel* and the original data to be retrieved, this technique is known as time-domain aliasing cancellation (TDAC). The IMDCT transforms *N* real numbers X_0, X_{N-1} into 2*N* real numbers y_0, y_{2N-1} is given as

$$\hat{x}(n) = \sum_{N=0}^{N/2-1} X(K) \cos\left[\frac{\pi}{2N}\left(2n + 1 + \frac{N}{2}\right)(2K + 1)\right] \qquad 7$$

where n=0, 1, 2.....N-1[9].

Channel Estimation Method

A wideband radio channel is normally frequency selective and time variant. For an OFDM mobile communication system, the channel transfer function at different subcarriers appears unequal in both frequency and time domains. Therefore, a dynamic estimation of the channel is necessary. Pilot-based approaches are widely used to estimate the channel properties and correct the received signal (Princen, 1986).

Figure 4 shows the block type pilot channel estimation. In the block type arrangement the pilot signal assigned to a particular OFDM block, which is sent periodically in time-domain. This type of pilot arrangement is especially suitable for slow-fading radio channels, because the training block contains all pilots, channel interpolation in frequency domain is not required. In block-type pilot based channel estimation, OFDM channel estimation symbols are transmitted periodically, in which all sub-carriers are used as pilots. If the channel is constant during the block, there will be no channel estimation error since the pilots are sent at all carriers (Bhoyar, 2012).

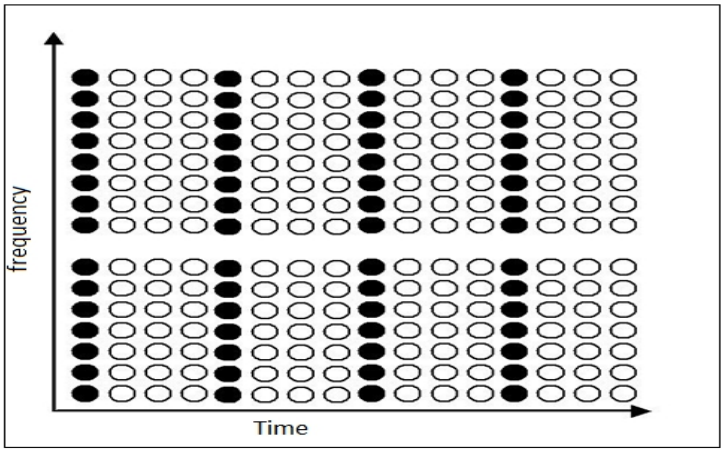

Figure 4. Block type pilot arrangement

Least Square Channel Estimation

In MIMO systems, the received signal is a superposition of N_t transmitted signals. Thus in order to deal with co antenna interference (CAI), channel estimation can efficiently use orthogonality between pilots to recover channel over all links. To carry out the DCT based channel estimation, the least square (LS) method has to be first applied to pilot sub-carriers. The channel estimated response at the *j*-th receive antenna is estimated by using the demodulated pilots signal (k) and the known pilot symbols (k) in the frequency domain. For WLAN transmissions using two transmit antennas and preamble symbols, we can write as follows,

$$\begin{cases} R_j(0) = \mathrm{diag}(X)H_{0j} + \mathrm{diag}(X)H_{1j} + E(0) \\ R_j(1) = -\mathrm{diag}(X)H_{0j} + \mathrm{diag}(X)H_{1j} + E(1) \end{cases} \quad 8$$

Where H_{ij} is the discrete response between the *i*-th transmit antenna and the *j*-th receive antenna. Without using any knowledge of the statistics on the channels, the LS estimators can therefore be estimated as,

$$H_{1j,LS} = H_{1j} + \frac{1}{2}\left(\left(\mathrm{diag}(X)\right)^{-1}E(0) + E(1)\right) \quad 9$$

$$H_{0j,LS} = H_{0j} + \frac{1}{2}\left(\left(\mathrm{diag}(X)\right)^{-1}E(0) + E(1)\right) \quad 10$$

It was observed that the accuracy of LS estimated channel response is degraded by the noisy component (Nguyen, 2004).

MDCT based channel Estimation

To improve the accuracy of the channel estimation, the DCT-based method has been proposed in order to reduce the noise component and the high frequency components in the transform domain (Kobayashi, 2004). Figure 5 illustrates the smoothing process using DCT. After removing the unused subcarriers, the estimated channel response given is first converted into the transform domain by the DCT algorithm and a smoothing filter is applied. After the smoothing, the IDCT is applied to return in the frequency domain. The channel impulse response in the transform domain is then given by the following equation 11,

$$h_{ij,LS,n}^{MDCT} = \sum_{N=0}^{N/2-1} H_{ij,LS,k} \cos\left[\frac{\pi}{2N}\left(2n + 1 + \frac{N}{2}\right)(2K+1)\right] \quad 11$$

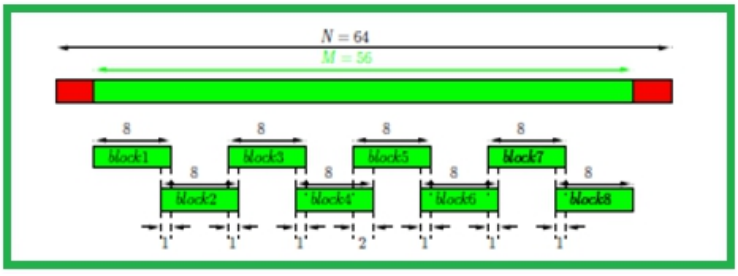

Figure 5. Smoothing of signal using DCT

The frequency channel response is given by

$$H_{ij,LS,k} = \sum_{N=0}^{n-1} h_{ij,LS,n}^{MDCT} \cos\left[\frac{\pi}{2N}\left(2n + 1 + \frac{N}{2}\right)(2K+1)\right] \quad 12$$

In order to reduce the complexity of the DCT based channel estimation, the whole DCT window will be divided into *R* blocks by using the lemma. If DCT windows are applied on N/R adjacent subcarriers among *M* in the frequency domain, useful energy of the corresponding channel impulse response will be concentrated on the first $2L/R$ samples in the transform domain. The principle of this approach is represented in Figure 6.

A DCT of size N/R is applied to each block and a smoothing filter of size $W = 2L/R$ is used for noise reduction. After the smoothing, the IDCT of size N/R is applied to return into the frequency domain.

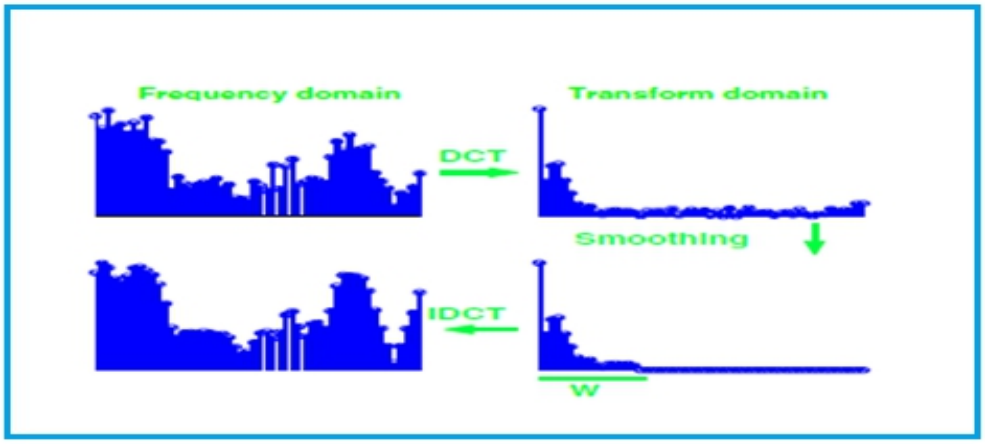

Figure 6. Separation of whole window into 8 blocks of size 8

In this approach there are two observations,

1. If we choose the size of the DCT blocks as a power of 2, the complexity will be significantly reduced by using some fast DCT algorithms,
2. The noise power is averaged on N samples instead of M in this approach. Thereby it presents a gain in comparison with the classical DCT based channel estimation.

Implementation of the proposed method

The flowchart represented in Figures 7 and 8 shows all phases of the channel estimation design and implementations. As shown in Figure 7, the binary data is given as input to the transmitter. The data to be transmitted on each carrier is modulated into a Quadrature Amplitude modulation format. The data on each symbol is mapped. In the simulations we used 16-QAM modulation. In order to identify the input from the different transmitter and for the least square channel estimation the pilot insertion is carried out.

After the required spectrum is worked out, an inverse discrete cosine transform is used to find the corresponding time waveform. The guard period is then added to the start of each symbol to avoid inter symbol interference. A Channel model is then applied to the transmitted signal. The model allows for the signal to noise ratio and multipath to be controlled. The signal to noise ratio is set by adding a known amount of noise to the transmitted signal (Li, 1999; Diallo, 2009).

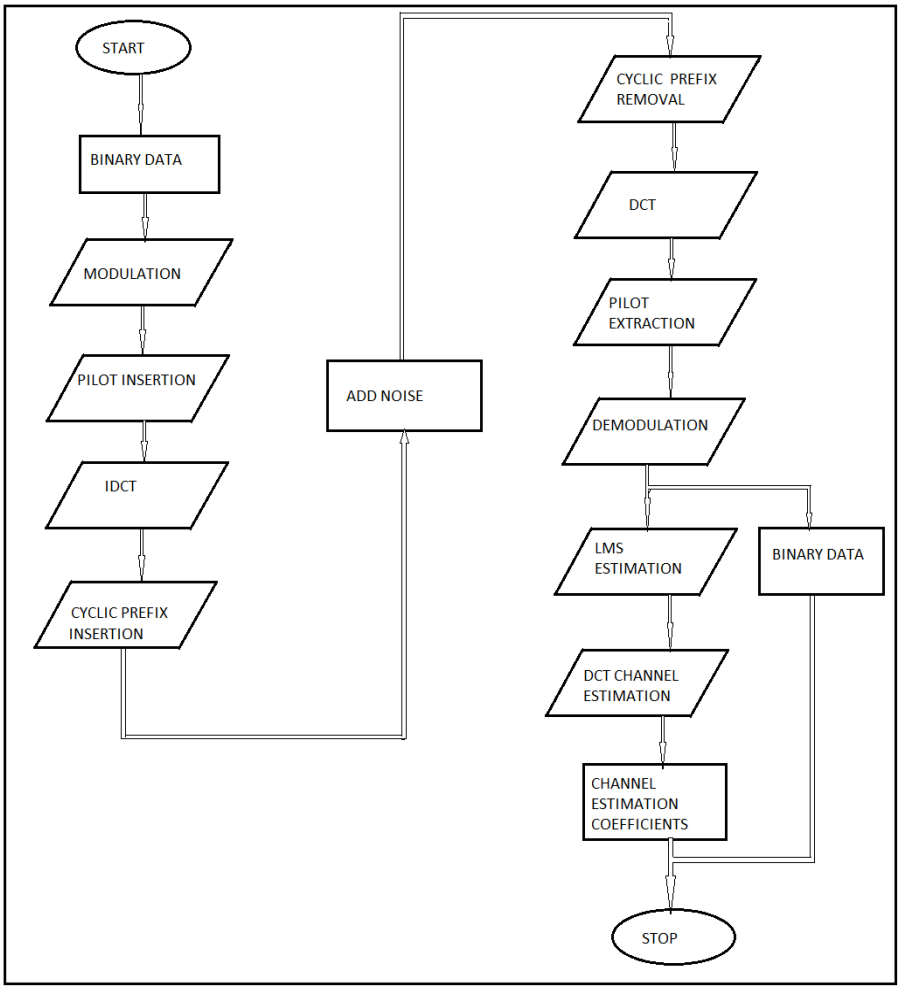

Figure 7. Flowchart of mimo-ofdm module

At the receiver side reverse operations are carried out. Inverse cyclic prefix is performed to remove the guard interval. Discrete cosine transform is performed to get corresponding frequency waveform. Later pilot extraction is performed to identify the respective transmitter and for the least square channel estimation. Least square channel estimation is used to calculate the channel estimation coefficients with less complexity. Since the least channel estimation cannot remove the error, discrete channel estimation with modified discrete cosine transform algorithm is used and channel coefficients are obtained with less complexity and high accuracy are obtained.

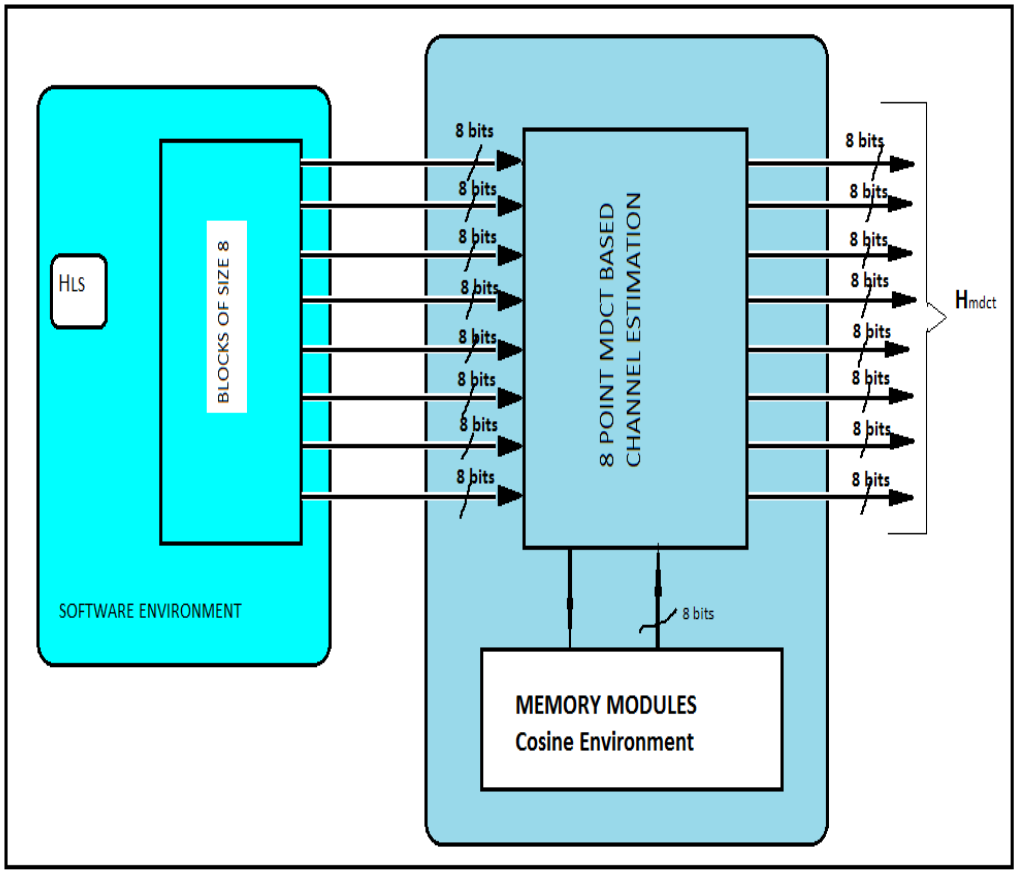

Figure 8. Flowchart of dct channel estimation

As shown in Figure 8, the input data (HLS) are found using software environment. After, the LS estimates are separated into 8 blocks of size 8 according to the principle detailed in the Figure 8. The cosine values defined are given as bit file which is stored in the memory module. One 8 points DCT based channel estimation (one IMDCT and one MDCT with the proposed Modified dct algorithm) is considered in this design. Therefore, as the number of output, the DCT estimated coefficients (HMDCT) will be obtained 8 by 8. The modified discrete transform algorithm is used in the DCT coefficient estimation. It is designed to be performed on consecutive blocks of a larger dataset, where subsequent blocks are overlapped so that the last half of one block coincides with the first half of the next block. This overlapping, in addition to the energy-compaction qualities of the DCT, makes the MDCT important for signal compression applications, since it helps to avoid artifacts stemming from the block boundaries. The design is simulated and validated using ModelSim which is a functional hardware

simulation. Thereafter, the Verilog source code is synthesized for Vertex 5 FPGA component.

Design Flow Using Verilog

The Figure 9 summarizes the high level design flow for an ASIC (i.e. gate array, standard cell) or FPGA. In a practical design situation, each step described in the following sections may be split into several smaller steps, and parts of the design flow will be iterated as errors are uncovered.

System-level Verification as a first step, Verilog may be used to model and simulate aspects of the complete system containing one or more ASICs or FPGAs. This may be a fully functional description of the system allowing the specification to be validated prior to commencing detailed design.

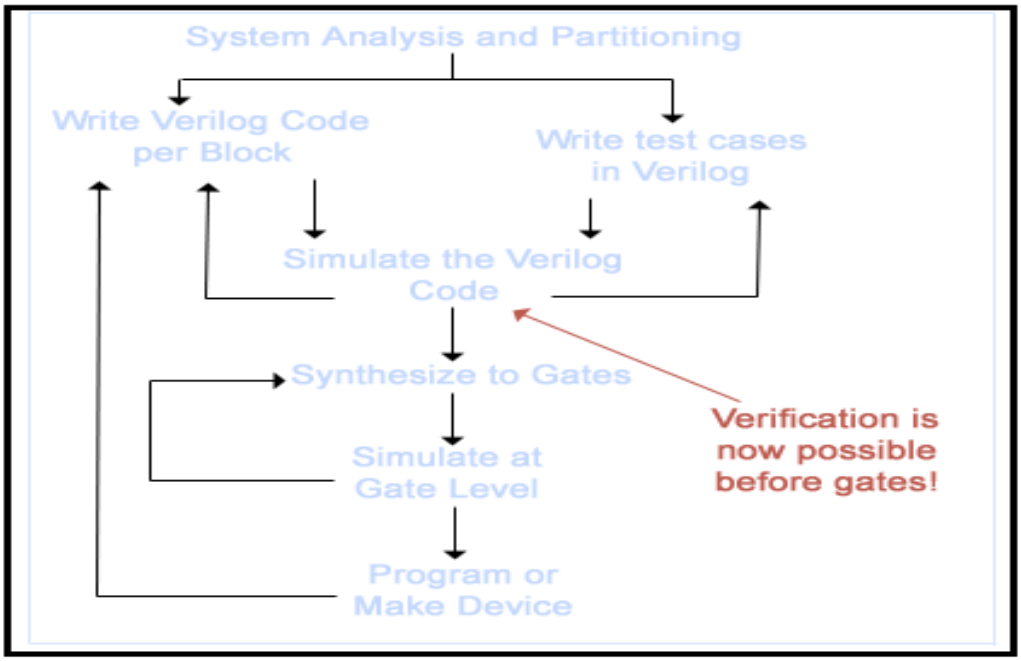

Figure 9. Design Flow of Verilog

RTL design and test bench creation

Once the overall system architecture and partitioning is stable, the detailed design of each ASIC or FPGA can commence. This starts by capturing the design in Verilog at the register transfer level, and capturing a set of test cases in Verilog. Test case generation is a major task that requires a disciplined approach and much engineering ingenuity: the quality of the final ASIC or FPGA depends on the coverage of these test cases.

RTL verification

The RTL Verilog is then simulated to validate the functionality against the specification. RTL simulation is usually one or two orders of magnitude faster than gate level simulation, and experience has shown that this speed-up is best exploited by doing more simulation, not spending less time on simulation.

Look-ahead Synthesis

Although some exploratory synthesis will be done early on in the design process, to provide accurate speed and area data to aid in the evaluation of architectural decisions and to check the engineer's understanding of how the Verilog will be synthesized, the main synthesis production run is deferred until functional simulation is complete.

Simulation flow

Creating the Working Library

In ModelSim, all designs are compiled into a library. Typically start a new simulation in ModelSim by creating a working library called "work". "Work" is the library name used by the compiler as the default destination for compiled design units.

Compiling Design

After creating the working library, compile the design units into it. The ModelSim library format is compatible across all supported platforms. So design can be simulated on any platform without having to recompile the design.

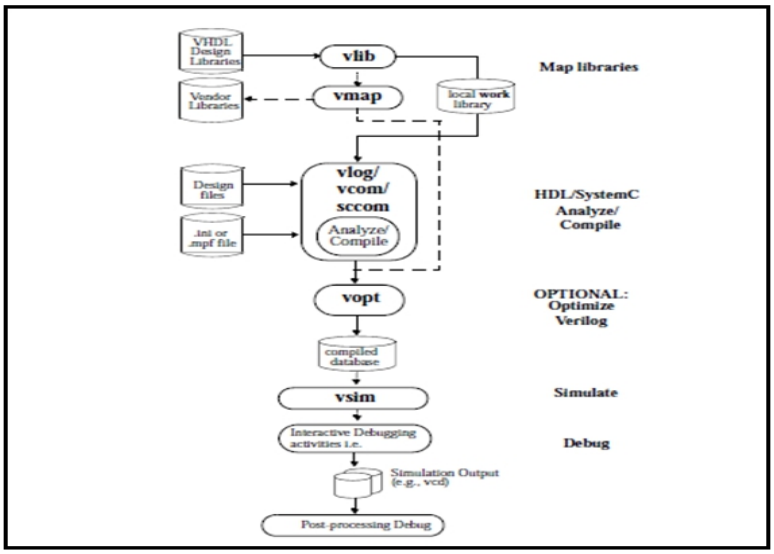

Figure 10. ModelSim tool structure

Loading the Simulator with Design and Running the Simulation.

With the design compiled, load the simulator with the design by invoking the simulator on a top-level module (VHDL) or a configuration or entity/architecture pair (VHDL). Assuming the design loads successfully, the simulation time is set to zero, and enter a run command to begin simulation.

Debugging Results.

If the results are not proper, then ModelSim's robust debugging Environment is used to track down the cause of the problem.

Results and Discussion

An MIMO-OFDM system is modeled using Xilinx ISE and ModelSim to allow various parameters of the system to be varied and tested. The aim of doing the simulations is to measure the performance of OFDM system under different channel conditions, and to check the complexity of MDCT channel estimation. The experimental results include synthesis results of MDCT and IMDCT in the form of design summary, RTL schematic, DCT, IDCT simulation results. It also includes the results of synthesis of whole MIMO-OFDM with power analysis and FPGA layout results.

The design is simulated and validated using ModelSim which is a functional hardware simulation. Thereafter, the verilog source code is synthesized forvertex5 FPGA component. The synthesis results are presented in the table,

Table 1: FPGA validated simulation output

Parameters	Results
LOGIC CELLS	830
PERIOD	4.346 ns
POWER	0.868 w

Figure 11 shows the simulation of DCT output. The percentage of device utilization in the simulation is estimated as in the figure. Similarly Figure 12 shows the simulation of IDCT output. The percentage of device utilization in the simulation is estimated as in the figure.

dct Project Status (06/15/2014 - 15:29:21)			
Project File:	FINAL.xise	**Parser Errors:**	No Errors
Module Name:	dct	**Implementation State:**	Synthesized
Target Device:	xc5vlx110t-2ff1136	**• Errors:**	
Product Version:	ISE 14.2	**• Warnings:**	
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1901	69120	2%
Number of Slice LUTs	2412	69120	3%
Number of fully used LUT-FF pairs	1332	2981	44%
Number of bonded IOBs	18	640	2%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48Es	20	64	31%

Figure11. Design summary of DCT

idct Project Status			
Project File:	FINAL.xise	**Parser Errors:**	No Errors
Module Name:	idct	**Implementation State:**	Synthesized
Target Device:	xc5vlx110t-2ff1136	**• Errors:**	No Errors
Product Version:	ISE 14.2	**• Warnings:**	127 Warnings (123 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1071	69120	1%
Number of Slice LUTs	1477	69120	2%
Number of fully used LUT-FF pairs	780	1768	44%
Number of bonded IOBs	23	640	3%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48Es	12	64	18%

Figure 12. Design Summary of IDCT

The signal is given input to the Resistor Transistor Logic circuit along with the clock signal. Figure 13 shows the simulation of RTL for DCT and IDCT.

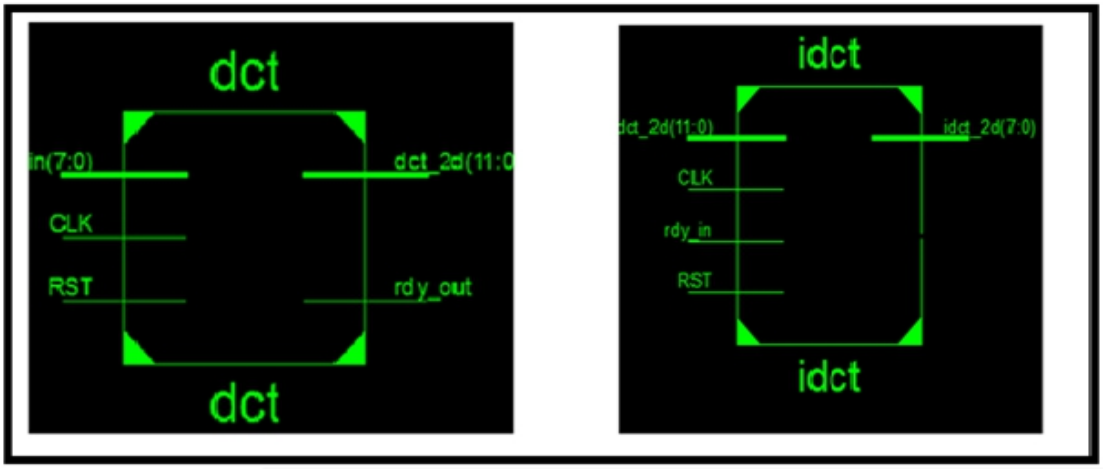

Figure 13. RTL Schematic representation of DCT and IDCT

The combined simulation output for combination of DCT_IDCT is as shown in Figure 14.

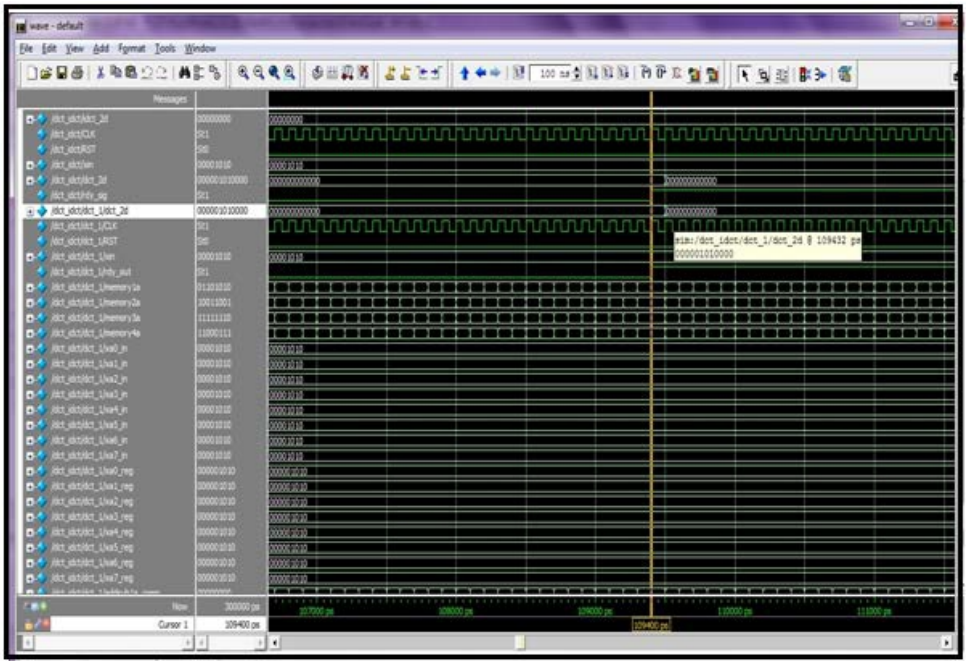

Figure 14. DCT_IDCT Simulation results

The RTL circuit for DCT_IDCT is shown in Figure 15.

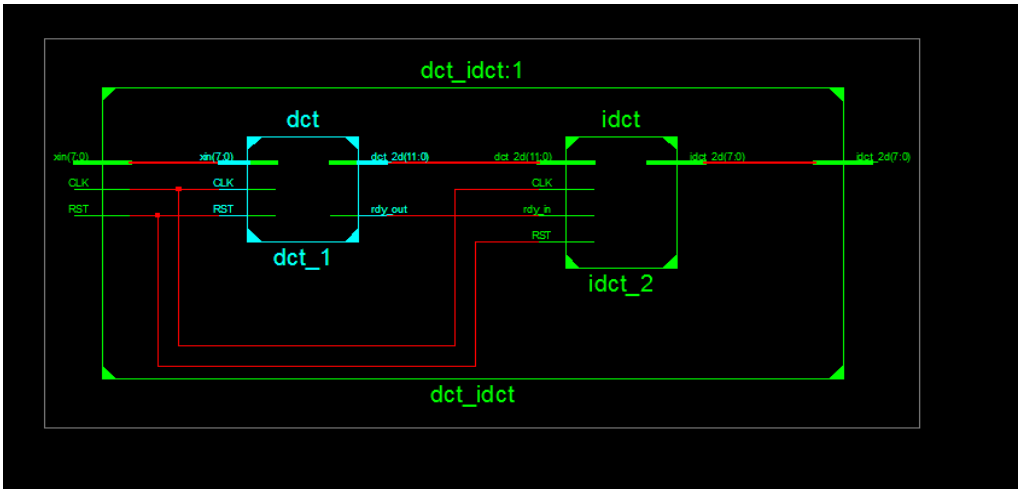

Figure15. RTL Schematic representation of DCT_IDCT

Figure 16 shows the simulation of MIMO-OFDM output. The percentage of device utilization in the simulation is estimated as in the figure.

mimo_ofdm_top Project Status (06/15/2014 - 16:32:49)			
Project File:	FINAL.xise	**Parser Errors:**	No Errors
Module Name:	mimo_ofdm_top	**Implementation State:**	Synthesized
Target Device:	xc5vlx110t-2ff1136	• **Errors:**	
Product Version:	ISE 14.2	• **Warnings:**	
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	830	20480	4%
Number of Slice LUTs	941	20480	4%
Number of fully used LUT-FF pairs	562	1209	46%
Number of bonded IOBs	23	360	6%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48Es	8	64	12%

Figure 16. Design Summary of MIMO-OFDM Top Module

Figure 17 shows the schematic representation of RTL circuit for MIMO-OFDM signal. The circuit consists of two RTL circuit for transmission and one for receiver.

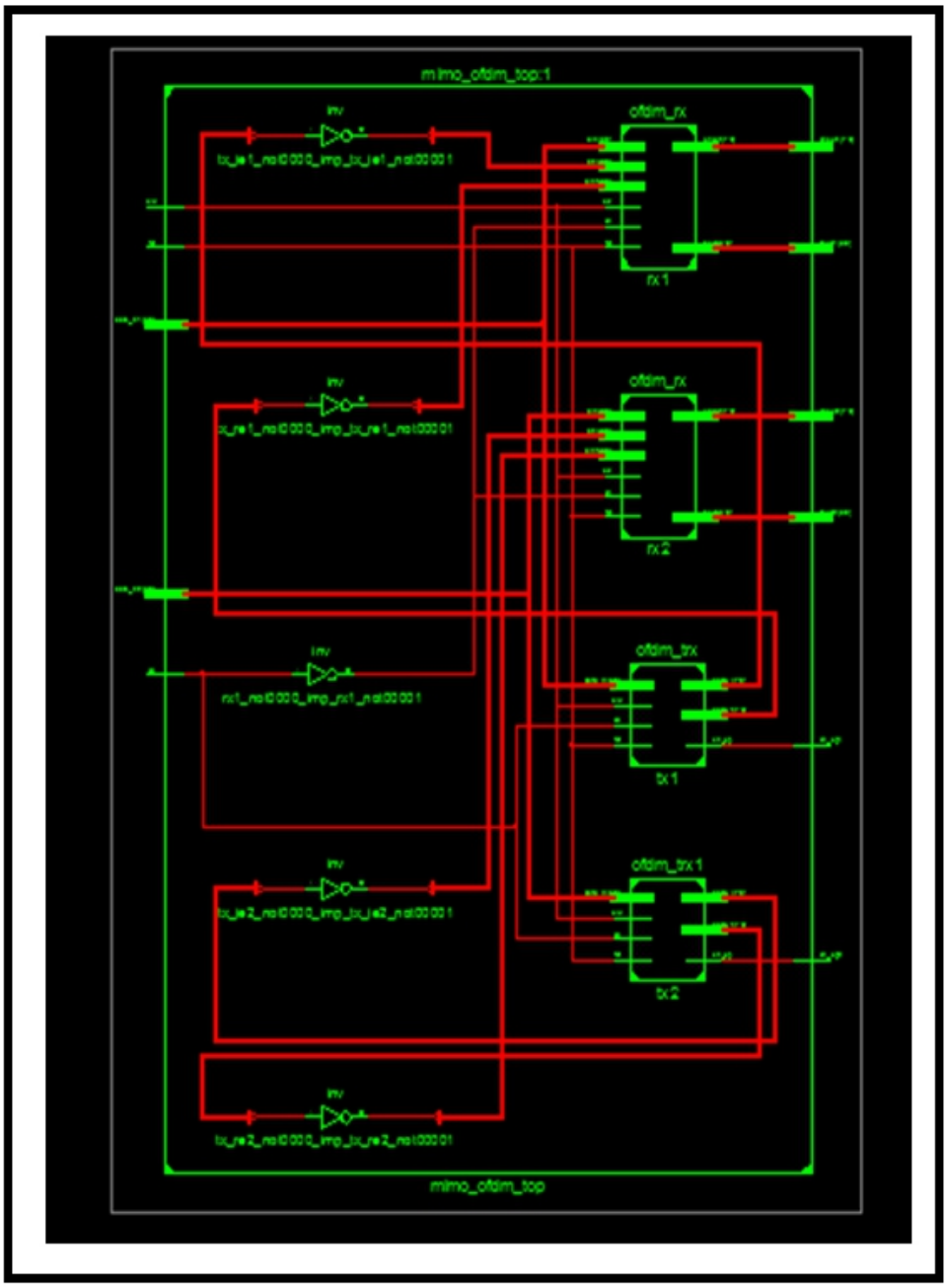

Figure 17. RTL Schematic representation of MIMO-OFDM Module

Figure 18 shows the simulation output of MIMO-OFDM transmission signal.

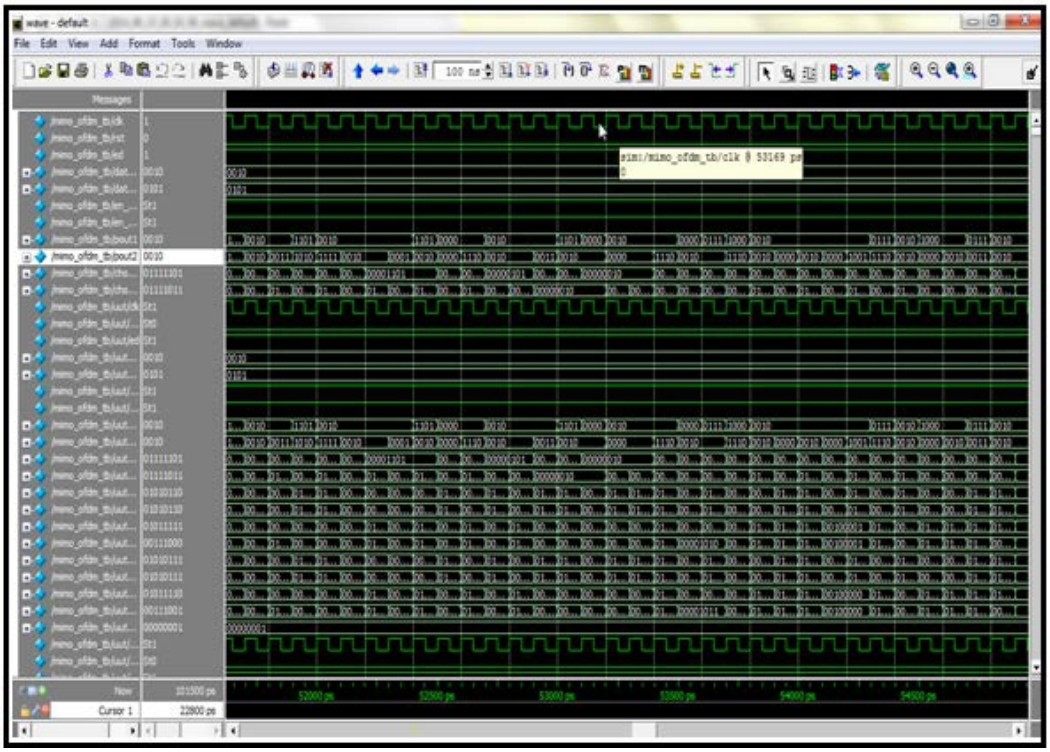

Figure 18. MIMO-OFDM simulation

The table for the asynchronous clock signal information is as shown in Figure 19. The maximum period for the transmission of the signal was 4.346 nano seconds.

```
Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 4.346ns (Maximum Frequency: 230.076MHz)
   Minimum input arrival time before clock: 1.454ns
   Maximum output required time after clock: 0.861ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)
```

Figure 19. Timing Summary for MIMO-OFDM

The power consumption for the transmission over the channel is analysed as shown in Figure 20. However, the overall output FPGA layout is as shown in Fgure 21.

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.120	281	--	--
Logic	0.000	20886	49152	42
Signals	0.000	27131	--	--
DSPs	0.000	140	512	27
DCMs	0.000	0	8	0
IOs	0.000	37	640	6
Leakage	0.748			
Total	0.868			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.531	0.100	0.431
Vccaux	2.500	0.091	0.000	0.091
Vcco25	2.500	0.002	0.000	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.868	0.120	0.748

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	6.2	79.6	55.4

Figure 20. Power Analysis For MIMO-OFDM

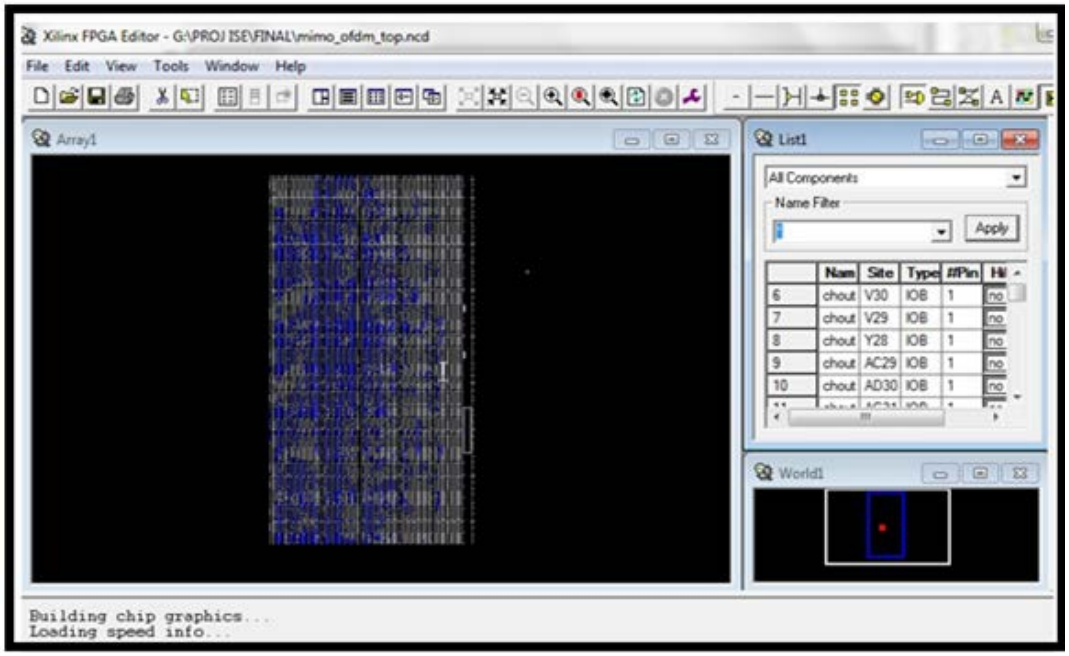

Figure 21. FPGA Layout For MIMO-OFDM

Conclusion

In this work, we have studied LSE and DCT estimators for channel estimation in MIMO-OFDM. The estimators in this study can be used to efficiently estimate the channel in an OFDM system given certain knowledge about channel statistics. High Signal to Noise Ratio can be obtained using the LSE estimator which is both simple and adequate. The LSE estimator has low complexity. For the error which cannot be removed completely using Least Square Estimator, further processing is carried out using DCT channel estimation. High accuracy is obtained using DCT channel estimation. Using the Modified Discrete Cosine transform algorithm low complexity has been achieved. The channel estimation module architecture is designed, synthesized and validated. The final synthesis results encourage the use of DCT based channel estimation for any coherent MIMO-OFDM system.

References:

Bhoyar, D. B., and Niranjane, V. B. (2012). Channel Estimation for MIMO-OFDM Systems. International Journal of Engineering Research and Applications (IJERA), 2(1), 044-050.

Chen, C. S., and Wong, W. S. (2006). A robust access protocol for wireless sensor networks. In Military Communications, IEEE Conference, MILCOM, pp. 1976-1981.

Coleri, S., Ergen, M., Puri, A., and Bahai, A. (2002). Channel estimation techniques based on pilot arrangement in OFDM systems. Broadcasting, IEEE Transactions on, 48(3), 223-229.

Colieri, S., Ergen, M., Puri, A., and Bahai, A. (2002). A study of channel estimation in OFDM systems. In Vehicular Technology Conference, 2002. Proceedings. VTC 2002-Fall. 2002 IEEE 56th, 2, 894-898.

Diallo, M., Rabineau, R., Cariou, L., and Hélard, M. (2009). On Improved DCT Based Channel Estimation with Very Low Complexity for MIMO-OFDM Systems. In VTC spring.

Diallo, M., Rabineau, R., Cariou, L., and Hélard, M. (2010). Transform Domain based Channel Estimation for 3GPP/LTE Systems. SCIYO. COM.

Kobayashi, H., and Mori, K. (2004). Proposal of OFDM channel estimation method using discrete cosine tramsform. In Personal, Indoor and Mobile Radio Communications, 2004. PIMRC 2004. 15th IEEE International Symposium on, 3, 1797-1801.

Li, Y., Seshadri, N., and Ariyavisitakul, S. (1999). Channel estimation for OFDM systems with transmitter diversity in mobile wireless channels. Selected Areas in Communications, IEEE Journal on, 17(3), 461-471.

Nguyen, V. D., and Pätzold, M. (2004). Least square channel estimation using special training sequences for MIMO-OFDM systems in the presence

of intersymbol interference. In Nordic Radio Symposium (NRS), Oulu, Finland.
Princen, J., and Bradley, A. (1986). Analysis/synthesis filter bank design based on time domain aliasing cancellation. IEEE Transactions on, Acoustics, Speech and Signal Processing, 34(5), 1153-1161.
Princen, J., Johnson, A., and Bradley, A. (1987). Subband/transform coding using filter bank designs based on time domain aliasing cancellation. In Acoustics, Speech, and Signal Processing, IEEE International Conference on ICASSP'87, 12, 2161-2164.
Wang, J., and Qiu, Y. (2012). A new DFT based channel estimation method for OFDM systems over multipath channels. In 2012 National Conference on Information Technology and Computer Science. Atlantis Press, 690-693.