DESIGN AND PERFORMANCE VERIFICATION OF CURRENT CONVEYOR BASED PIPELINE A/D CONVERTER USING 180 NM TECHNOLOGY

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Abstract

This paper reports a design and performance verification of pipeline Analog to Digital Convertor (ADC) using a second generation current conveyor for increasing accuracy, bandwidth and decrising power desipation of an ADC. The current conveyor used in this design is based on the CMOS inverter which works in transconductance mode rather than traditional current conveyor so that the low voltage operations would also be carried out easily, which makes the ADC more versatile. Extensive simulations along with performance evaluation of ADC are done to check the operating frequency range and band width. Results are reported that shows the capability and effectiveness of the proposed design. Authors have verified the capability of this design to operate over the high frequency range (1 Hz to 100GHz). Best simulation results obtained on cadence environment with 180nm technology. Also the layout design is carried out in the cadence virtuoso environment and verified the performance of the proposed design. Finally results of complete ADC design is reported.

Keywords : current conveyor, CMOS inverter, resolution, cadence, bandwidth, layout , LVS

Introduction

ADCs are rarely used alone, but are often included in more elaborate systems. The performance of the ADCs will affect the performance of the system where it is included and the precision with which the ADC parameters are known is necessary to compute the precision of the final result of the system using it. The rapid growth of the signal processing applications is driving the pipelined ADC design towards higher speed, higher precision, lower power consumption, lower supply voltage, smaller size and higher levels of integration along with the advancement of the fabrication technology. While continual speed improvement can still be achieved by using the advanced sub-micron or deep sub-micron CMOS processes, data converter designers find it more and more difficult to improve or even keep the accuracy of pipeline ADCs which reply on high gain operational-amplifier (OPAMP) and well matched components to produce high-precision converters. The continuing trend of submicron CMOS technology scaling, which is coupled with lower power supply voltages, makes it possible to keep up with the application development. At low power supply voltage, large open-loop OPAMP gain is difficult to realize without sacrificing bandwidth and/or power consumption [1]. As a result, the finite OPAMP gain is becoming a major hurdle in achieving both high speed and high accuracy in following ways.

First, large open loop OPAMP gain is difficult to realize without sacrificing bandwidth given the continuing trend of submicron CMOS scaling which is coupled with lower power supply voltages. Second, there are some physical limits on the component matching due to process variation, so it cannot be improved continually with CMOS technology scaling. Thus, while the state-of-the-art pipelined ADCs has exceeded 100MS/S (mega-samples-per-second) in CMOS technology [2-4]. The commonly achieved resolution is still bound within the range of 8-12 Effective-Number-of-Bits (ENOBs) due to the limitations set by component mismatches and finite OPAMP gain. Use of multi-bit-per-stage architecture and design optimization can achieve 14-bit performance as demonstrated in [5] but most pipelined ADCs with more than 12-bit resolution will usually require some kind of linearity enhancement techniques. Also the switched-capacitor (SC) circuits are usually used in pipeline ADCs not only they can construct the S/H circuit but also for the MDAC circuit. The SC circuit is usually made by OPAMP, for this reason, the accuracy of the OPAMP always determines the SC circuit performance. The second generation current conveyor has higher accuracy and wider frequency ranges, hence the CC-II- based circuits are popularly used in many applications like filters oscillators and so on. Basic architecture of the proposed design is given in Figure 1.
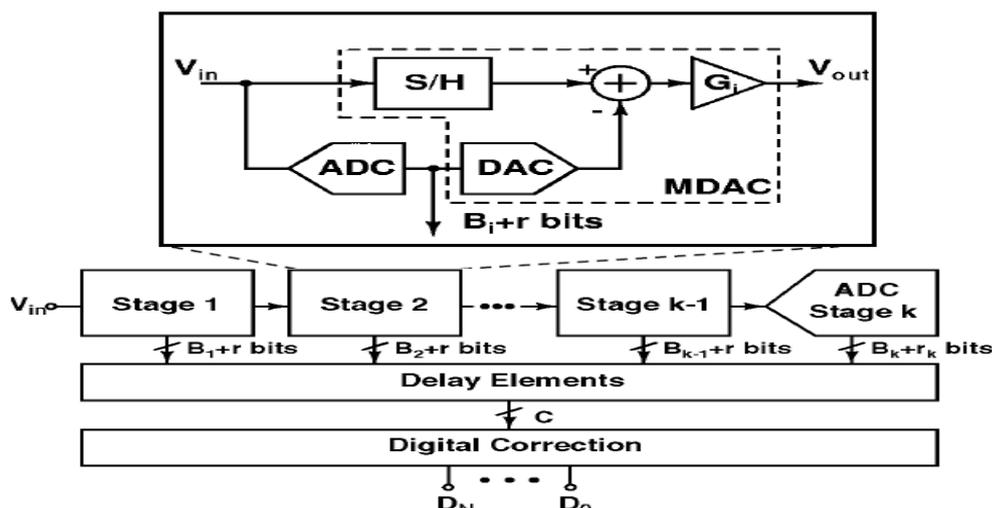
Figure 1 Basic architecture of a pipeline ADC

Design of an ADC

Design of CMOS inverter based second generation current conveyor

Current conveyor second generation (CCII) has attracted the attention of researchers in the field of active filters and oscillators due to its distinct advantages over operational amplifier. This is attributed to their larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry and low power dissipation [6-9]. Current mode circuits play the very important role in the design of various analog signal processing circuits. The main types of current mode circuits are current conveyor, operational transconductance amplifier, current feedback operational amplifier etc. Current conveyor circuits offer many advantages over voltage mode circuits to be used in the various analog signal processing circuits like large bandwidth, less complex, wider voltage and current swing. Figure 2 shows the proposed schematic of the CMOS Based second generation current conveyor.
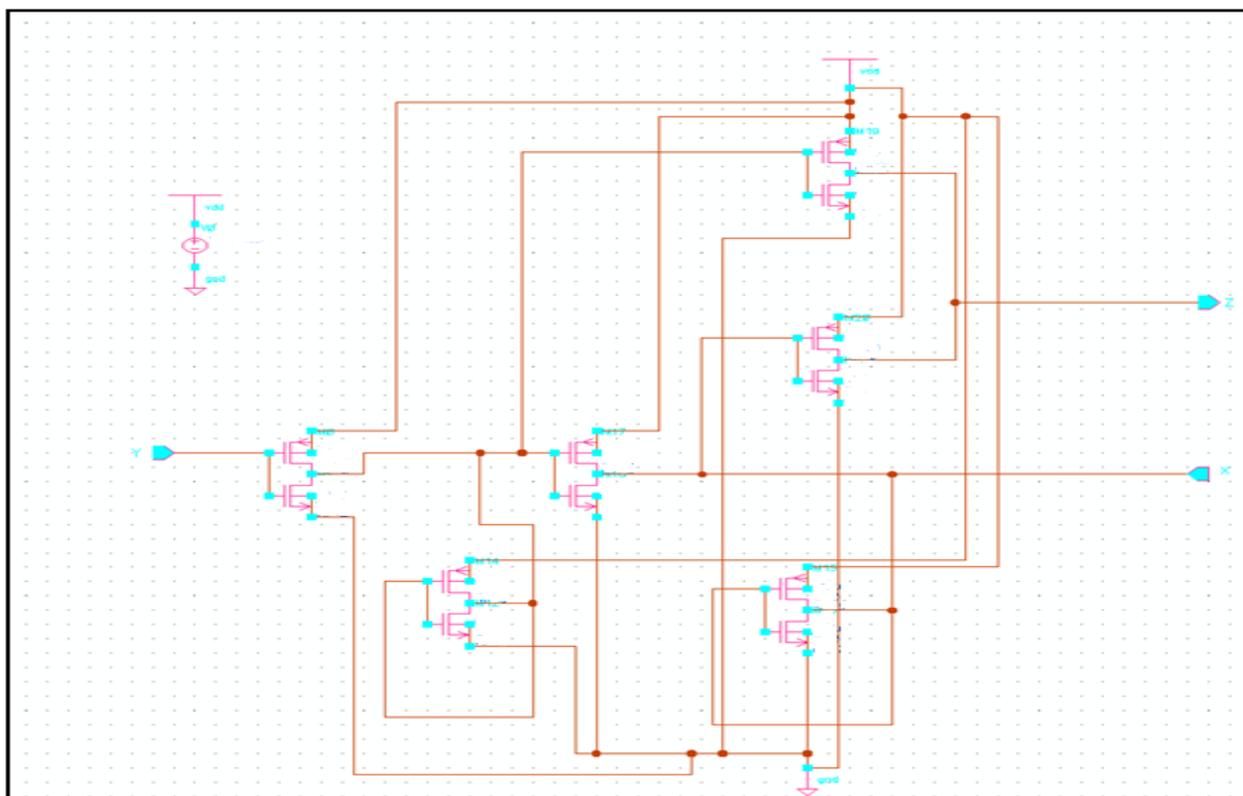
Figure 2 Schematic view of Proposed Current Conveyor

After that authors have done work using this current conveyor and designed different circuits like: sample and hold circuit, multiplying D/A converter and comparator and simulate all the design in cadence environment using 0.18µm technology. Here only presenting main blocks of the design. MDAC and comparators are very important section for ADC.

Design of a Multiplying Digital to Analog Converter

Figure 3 shows the schematic of the MDAC using proposed CC-II. In this feedback capacitor C2 plays a major role between terminals X and Z to cancel the high frequency and switching noises. When the voltage at the terminal Y changes, the voltage of the terminal X will follow that of the terminal Y and the settling time is faster due to feedback capacitor. The value of the feedback capacitor is 1pf.

It is very clear from the schematic that the switches are implemented using transmission gate having PMOS and NMOS of particular size so that the switch resistance does not affect the working of the MDAC circuit. The inverting and non inverting clock signal is provided using the inverter preceded by the pulse Input (Vp)
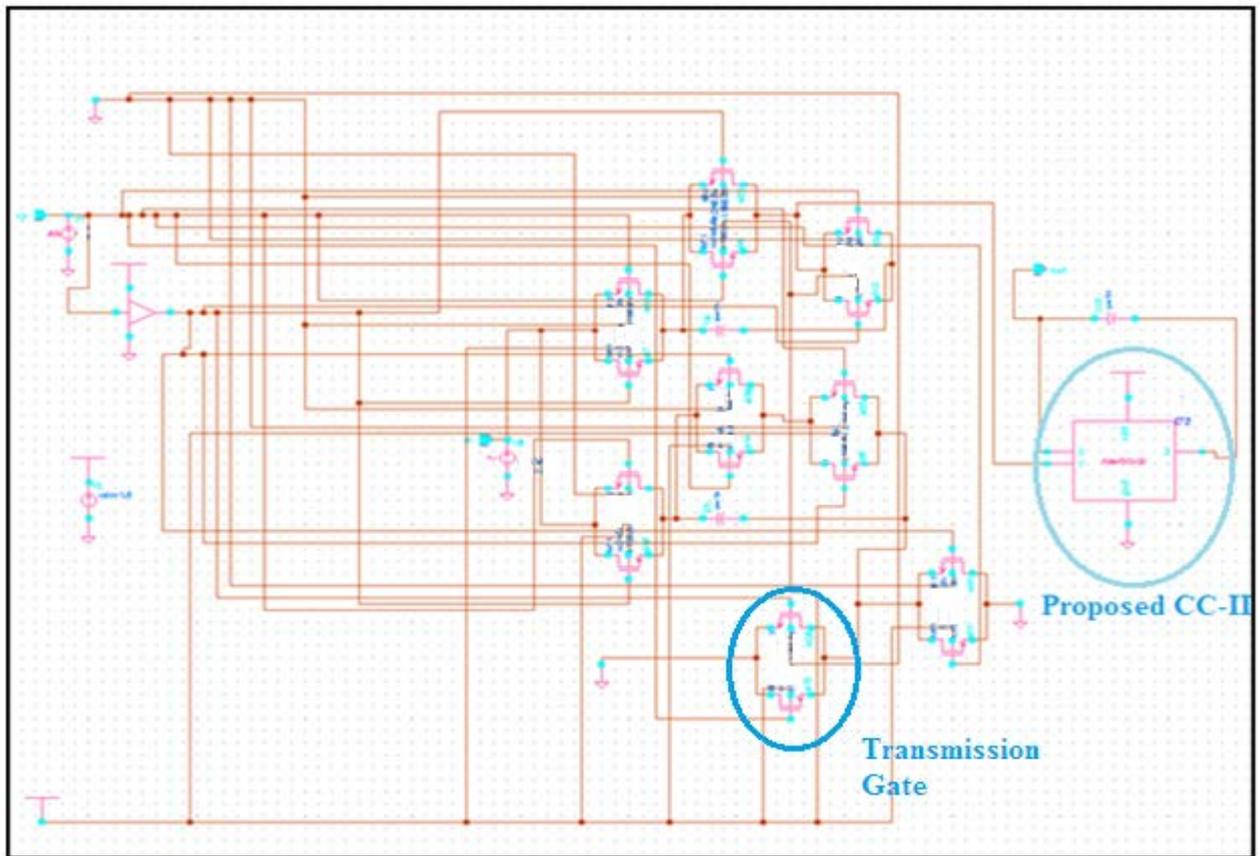
Figure 3 Schematic of MDAC circuit

Design of a comparator

Figure 4 has given a schematic view of a comparator design based on figure 2. This is a voltage comparator and it has consist of three main stages as shown in schematic view i.e. Preamplifier Stage, Decision Circuit and Output buffer stage. In the preamplifier stage the bias current (I_{bias}) is of 20uA which is used to bias the transistor M1 and M2; from the schematic circuit it is clear that:

$$io^+ = \frac{gm}{2}(v^+ - v^-) + \frac{Ibias}{2} = Ibias - io^-$$

(1)

Where io^+ is positive branch current

io^- is negative branch current

v^+ is non inverting input

v^- is inverting input

g_m is transconductance of two input transistor

$$gm = \sqrt{2\beta ID}$$

(2)

Where β is process technology parameter

I_D is the drain current through the input transistor

Using above equations we can decide the value of the aspect ratio of the transistors of the preamplifier circuit as:

M1= 900n/180n M2= 900n/180n M3= 270n/180n

M4= 270n/180n M5= 270n/180n M6= 270n/180n

The decision circuit uses the positive feedback from the cross gate consists of M7, M8, M9, M10 to increase the gain of the comparator circuit. The current io+ and io- from the preamplifier stage is provided as the input to this circuit, if io+ >> io- then M7 and M9 are ON but M8 and M10 are OFF.

$$\beta7 = \beta10 = \beta A \ \& \ \beta8 = \beta9 = \beta B$$

(3)

Where β's are process technology parameter of the transistor

$$\beta = \mu n Cox(\frac{W}{L})$$

(4)

If the above given condition fulfills then the output voltages vo⁻ and vo⁺ through the decision circuit are:

$$vo^- = 0$$

(5)

$$vo^+ = \sqrt{\frac{2io^+}{\beta A}} + vthn$$

(6)

where v_{thn} is the threshold voltage of the NMOS.

Voltage across M9 reduces v_{thn} & then the M9 enters into the saturation region, then the current through M9 i.e. io- will be:

$$io^- = \frac{\beta B}{2}(vo^+ - vthn)^2 \tag{7}$$

$$io^- = \frac{\beta B}{\beta A} io^+$$

(8)

This is the point at which switching takes place if βA = βB then io+ = io-

To shift the output of the decision circuit up to 1V the MOSFET M11 is added in series with the decision circuit. The comparator circuit has used an output buffer self biasing differential amplifier, an inverter was added on the output amplifier as an additional gain stage and also used to isolate any load capacitances.
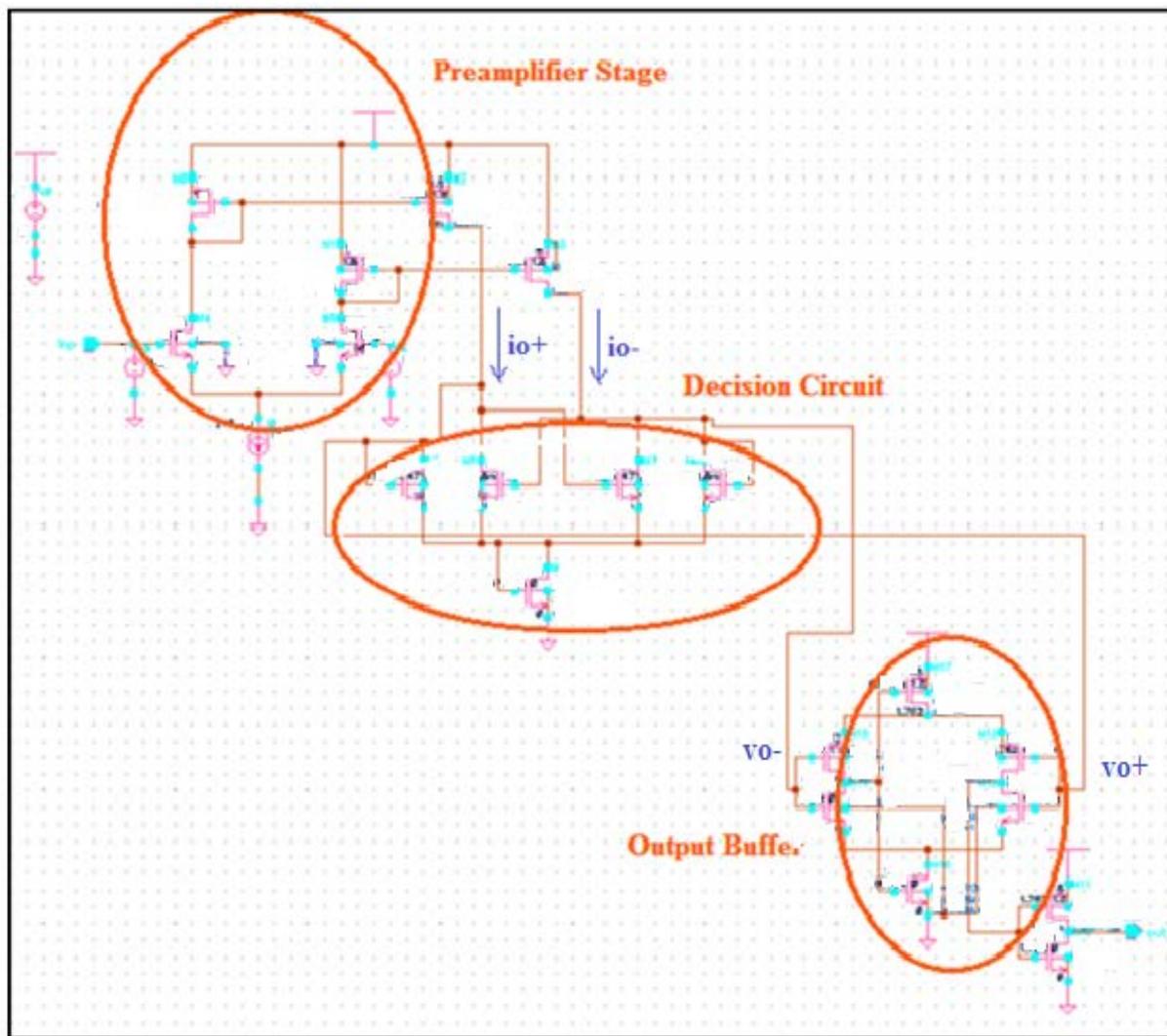
Figure 4 Schematic of Comparator circuit

Design of 8-bit Pipeline ADC

In this authors have designed a 8 bit pipeline ADC based on single stage pipeline ADC. In the schematic design a 6 bit pipeline ADC is connected with two single stage pipeline ADC. Figure 6 shows a schematic view of 8 bit ADC. After completion of schematic, authors have implemented layout of the complete ADC. Than checked DRC and LVC of the design and no error found as shown in figure 7.
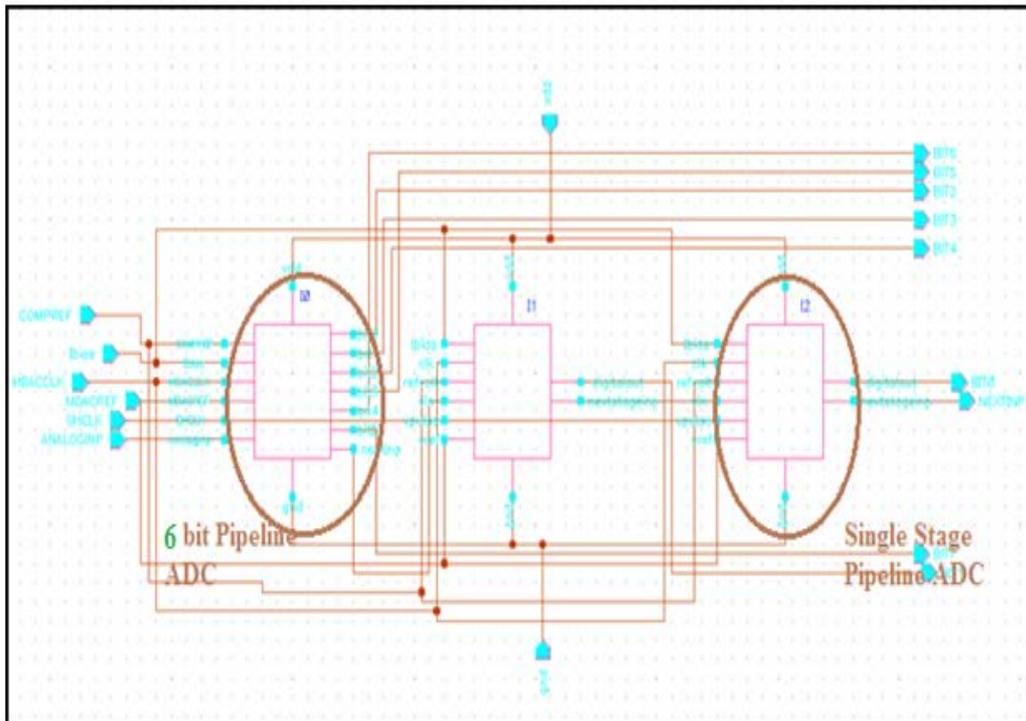
Figure 5 Schematic of 8 bit Pipeline ADC
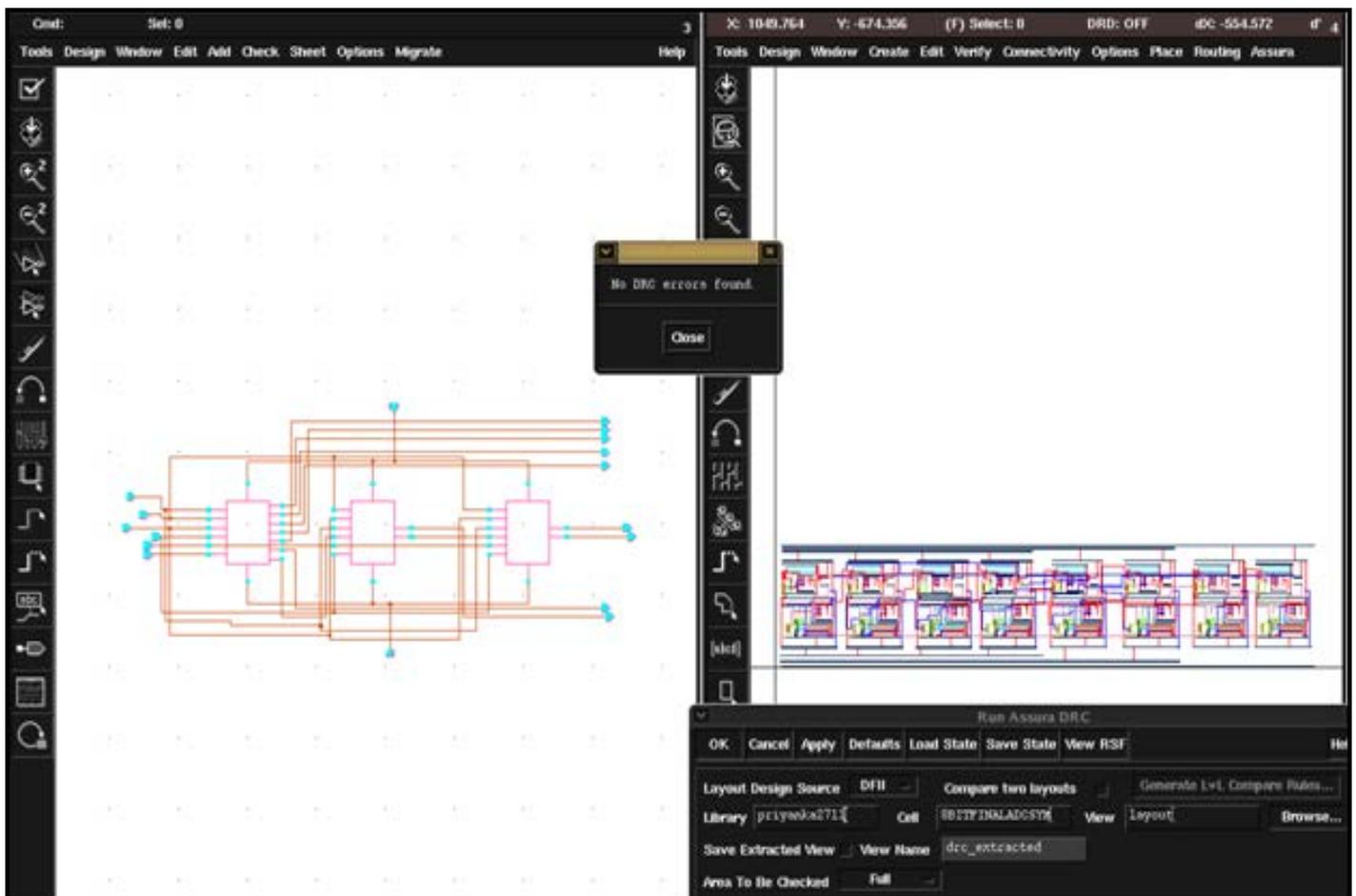
Figure 6 Layout of the proposed 8 bit Pipeline ADC

Simulation results and discussion

Simulation on cadence is done for testing and determining outputs of various stages of the design. Figure 7 present the sampled and hold block output of the proposed pipeline ADC, the provided clock frequency for sampling is 16 MHz and the input frequency was 2 MHz, the sample and hold outputs are taken from terminals X and Z respectively. The measured parameters are given in table 1.

Table 1 Parameters of the proposed Sample & Hold Circuit

S.NO.	PARAMETER	VALUE
1	Sampling Frequency	50 MHz
2	Sample time	10 ns
3	Hold time	15 ns
4	Load capacitance	1 pF
5	O/P Highest Amplitude	2.05 V
6	O/P Lowest Amplitude	0.7 V
7	Power dissipation	3098.29 uw
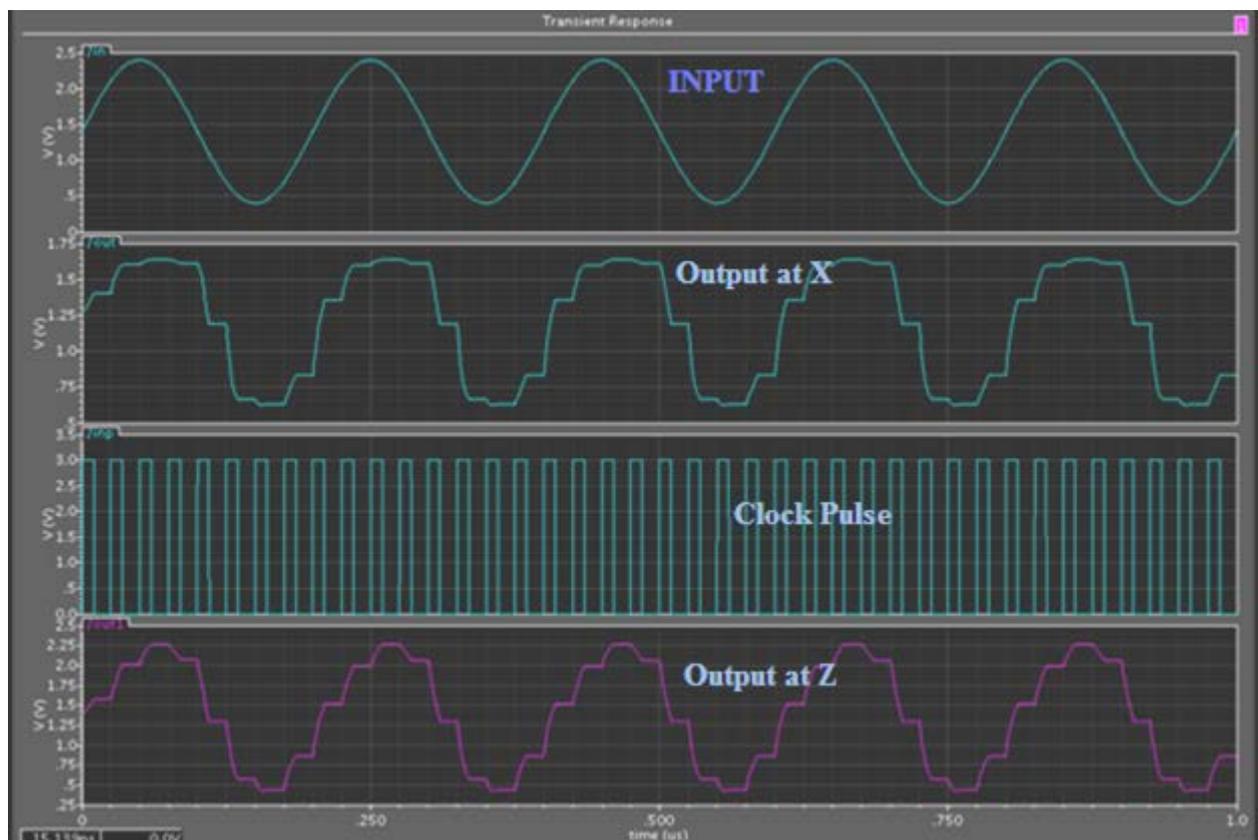
Figure 7 Input and Output waveform of the sample & hold circuit

The output is determined by two terminals X and Z with the same current to make the output voltage settling faster.
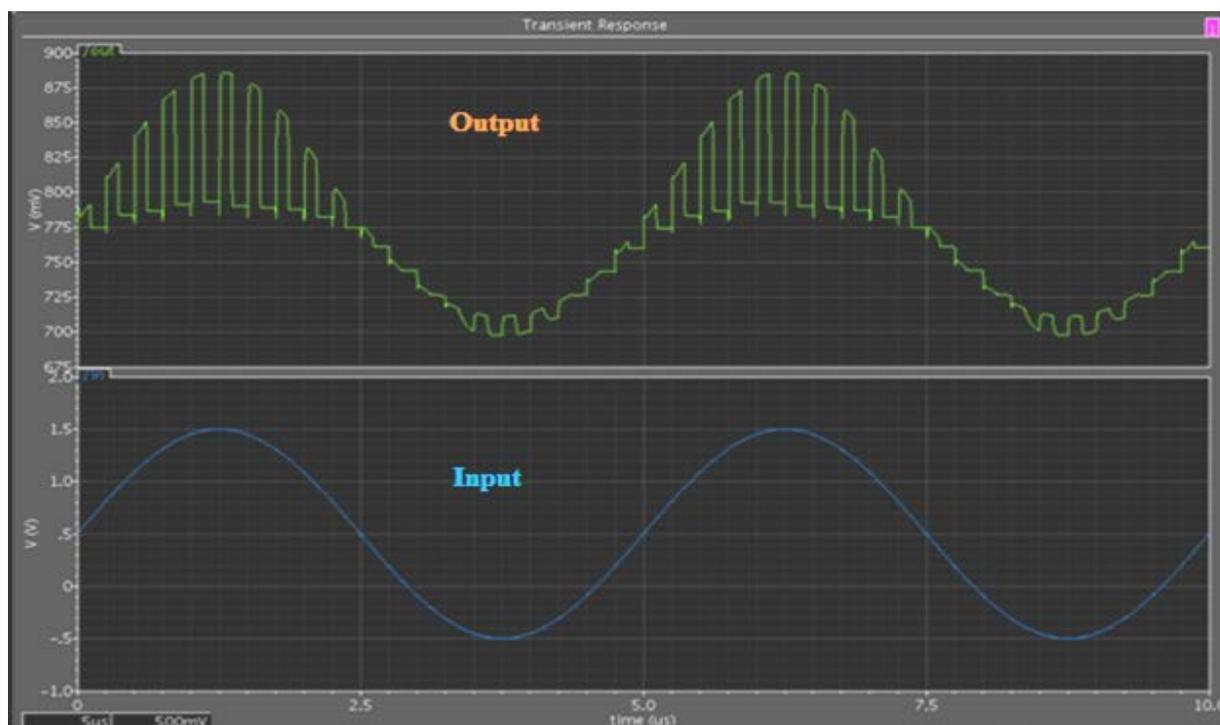
Figure 8 Input and Output waveform of MDAC for sinusoidal input

Figure 8 gives the input/output waveform of the MDAC for sinusoidal input, the sinusoidal wave is applied at the input with 0.5 V $_{p-p}$ at 2MHz (the MDAC operates at amplification mode i.e. reference of MDAC is 0 V. During this process authors have calculated some important parameters as given in table 2.

Table 2 Parameters of the proposed MDAC Circuit

S. No.	Parameter	Value
1	Settling time(Without C F/B)	97 nsec.
2	Settling time(With C F/B)	71 nsec.
3	Power Dissipation	542 uW

Comparator Gain Plot

Figure 9 shows comparator gain plot, which shows the gain, is about 2076. This can be calculated by performing the DC analysis of the comparator design i.e. by plotting the output by fixing the reference voltage and varying the input. At this stage author have determined different parameters like: comparator gain, power dissipation, offset voltage, settling time and conversion Time. Parameter values are given in table 3.

Table 3 Parameters of the proposed Voltage comparator

S.No.	Parameter	Value
1	Comparator Gain	2076
2	Power Dissipation	78.26uW
3	Offset Voltage	1.1mV
4	Settling Time	48ns
5	Conversion Time	0.865 nsecs
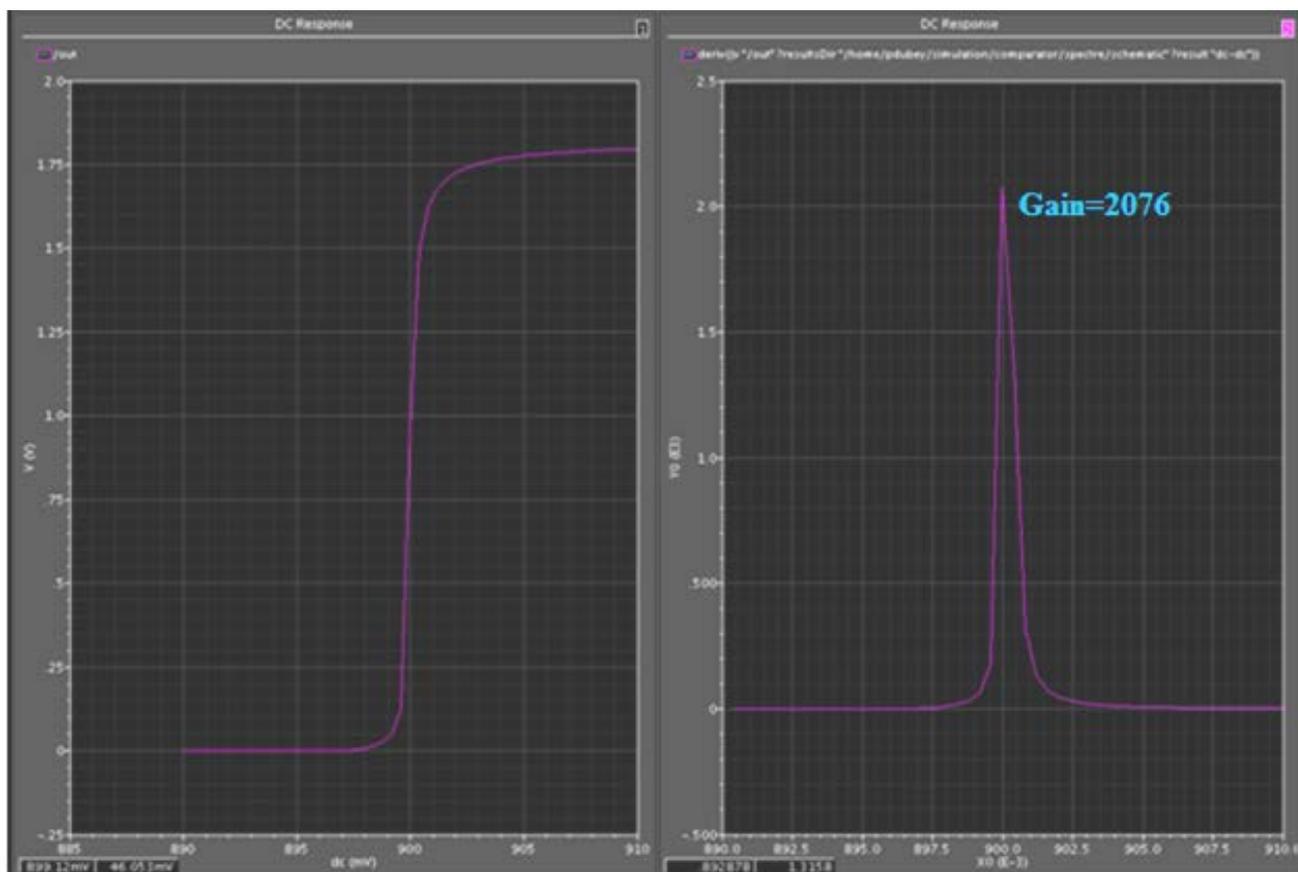
Figure 9 Transfer Curve and Gain Plot of Voltage comparator

Results of 8-bit Pipeline ADC

Finally 8 bit pipeline ADC is designed and simulated in cadence environment with 0.18µm technology. Figure 10 shows the transient response of the 8 bit ADC for the exponential input of 1.8 V. Output starts with one value and its rise time starts at 0 second and constant at 50 nsec., fall time start at 50nsec. and constant at 500nsec. The complete circuit has the power dissipation is 14.2 mW. Table 4 has given various measured parameters.
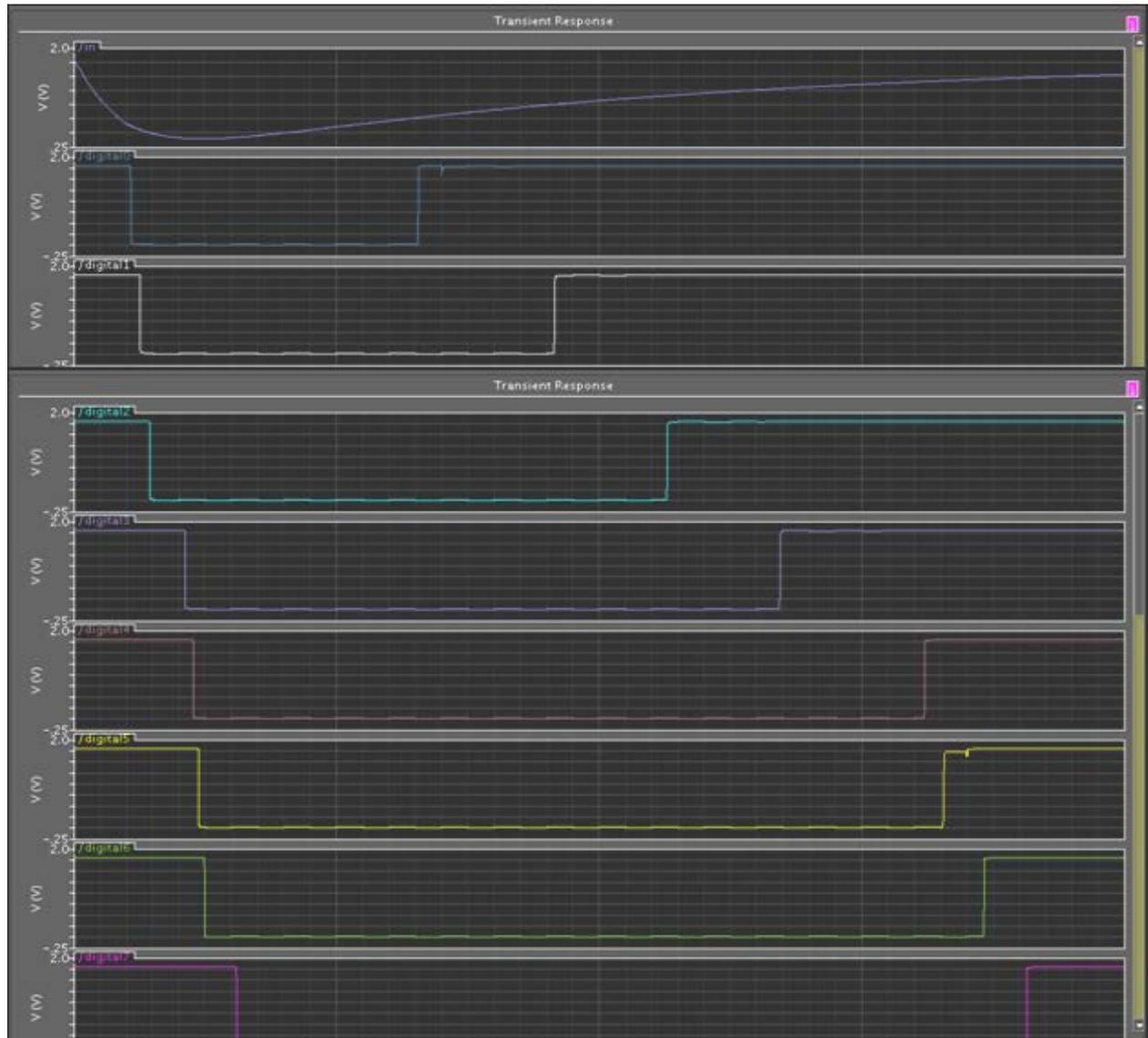
Figure 10 Output of the 8-bit Pipeline ADC

Table 4 Final results of a proposed pipeline ADC

Parameter	Used parameter values	Measured/estimated values with proposed design	
Technology	0.18 um CMOS	Power dissipation	14.2 m W
Power Supply	1.8 V	Area	1.12 mm^2
Sampling frequency	25MHz	Estimated Resolution	7.66 bits
Resolution	8 bit	SINAD	47.8932 db
		$(S/N)_{ideal}$	49.92 db
		INL	1.2 LSB
		DNL	0.82 LSB

Conclusion

An area and power-efficient current conveyor pipelined ADC is reported in this work. Propoesd ADC employs the use of current conveyor in place of the OPAMP; also in place of the traditional current conveyor CMOS inverter based current conveyor is designed and used. The circuit techniques such as the use of Multiplying DAC enhance the applications of the proposed design in the area efficient application. The proposed architecture is implemented in a 180nm digital CMOS technology with standard threshold voltage devices only. The presented pipelined ADC design is compact in size as compared with other ADCs with similar sampling rates and resolutions. This design has achieved the best power efficiency and power consumption about 14.2 mW under a 1.12 V supply. Also estimated the parameters of the design with implemented algorithms as given in table 4.

Acknowledgement

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