EFFECT OF THRESHOLD VOLTAGE AND CHANNEL LENGTH ON DRAIN CURRENT OF SILICON N-MOSFET

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Abstract

This paper investigates the effect of threshold voltage on drain current for different channel lengths and analyses the impact of short channel on threshold voltage for Silicon n-MOS at room temperature. For characterization, n-MOS model N08 is used where the short channel length and width of 0.8μm and 10μm and long channel length and width of 20μm and 200μm are chosen. The simulation is accomplished using LTSPICE and the data is analysed and characterized using MatLab. For both cases it is found a significant increase in drain current. Therefore, threshold voltage and channel length has substantial effect on drain current i.e. on device I_d-V_{ds} and I_d-V_{gs} characteristics.

Key Words: Channel Length, Drain Current, Threshold Voltage, MOSFET

Introduction

The threshold voltage (V_{th}) and channel length (L) are two important parameters for modeling and characterization of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) (Schroeder, 2006; Conde, Sánchez & Liou, 2000). Several definitions of threshold voltage have been mentioned in the literature (Benson et al., 2001) but it is usually understood as the gate voltage at which an inversion layer forms at the interface between the insulating layer and the substrate of the transistor. The purpose of the inversion layer's forming is to allow the flow of electrons through the gate-source junction. Therefore, threshold voltage represents the onset of significant drain current flow which also depends on channel length. In addition, threshold voltage plays an important role for the determination of device operation regimes which can be divided into three operational regions (Dunga et al., 2006). First, if the threshold voltage is less than the gate voltage (V_{gs}), the inversion charge density is large enough to operate the device in the strong inversion region where drift current is dominant.

Second, if V_{th} is greater than V_{gs}, the inversion charge density is smaller than substrate doping concentration which compels the device to operate in the weak inversion region so diffusion current becomes dominant (Muller, Kamins & Chan, 2013). Lastly, if V_{th} is very close to V_{gs}, the inversion charge density is such that the device operates in the transition region where both diffusion and drift currents are important. There exist various methods to determine the value of threshold voltage (Zhou, Lim & Lim, 1999). Among the available procedures to determine V_{th}, the measurement of static transfer characteristics (I_d-V_{gs}) of a single transistor exhibits greater part (Sánchez et al., 2002). Most of these methods use the strong inversion region (Tan, Xu & Wang, 2000) whereas very few consider the weak inversion region (Aoyama, 1995). In this experiment the threshold voltage is varied for short channel and long channel n-MOSFET and the effect on drain current is observed. Also, the threshold voltage is analyzed from I_d-V_{gs} characteristics curve for short channel operation.

Device Modeling

The devices with channel length much greater than the sum of drain and source depletion widths are regarded as long channel MOSFET where edge effects can be neglected. On the other hand, a MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion layer widths of the source and drain junction. The basic structure and layout of an n-channel MOSFET are shown in Fig. 1(a) and 1(b) respectively.

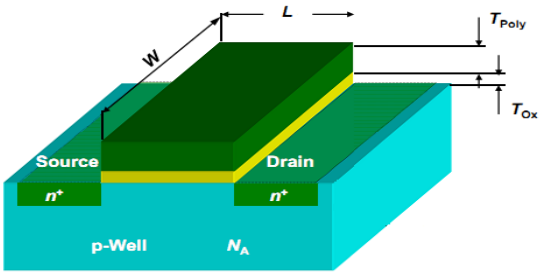

Fig. 1(a): Structure of the N-MOS

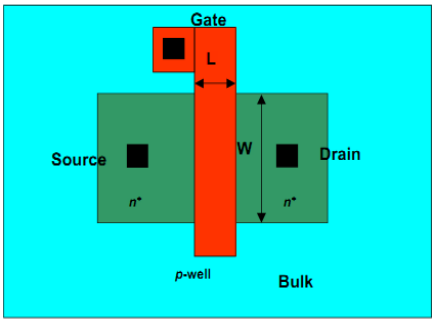

Fig. 1(b): Layout of the device

In the necessity to obtain higher performance regarding speed, functionality and chip density, the channel length (L) and channel width (W) are being down scaled (Sakurai & Newton, 1991). But as the device scaling makes the channel length less than a micron (L < 1μ), second order effects that were ignored for long channel devices become prominent i.e. so called short channel effect arises. Therefore, modification of the threshold voltage is necessary due to short channel effects at zero bias condition.

For n-channel MOSFET with n^+ polysilicon gate and p-type silicon substrate the threshold voltage at zero-bias is defined as (Peng & Ismail, 2007)

$$V_{TO} = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_{Si} q N_A (2\phi_F)}}{C_{ox}} \quad (1)$$

where ϕ_F is the Fermi potential given as

$$\phi_F = \frac{kT}{q} ln\left(\frac{N_A}{N_i}\right) \quad (2)$$

k is the Boltzmann's constant, N_A is the substrate doping concentration, ε_{Si} is the dielectric permittivity of silicon, q is the electronic charge and C_{ox} is the gate oxide capacitance. The flat band voltage V_{FB} is given as

$$V_{FB} = \left(\phi_{ms} - \frac{Q_{ss}}{C_{ox}}\right) \quad (3)$$

where ϕ_{ms} is the metal-semiconductor work function difference and Q_{ss} denotes the fixed oxide charge.

Equation (1) is accurate in describing large MOS transistors, but it collapses when applied to small-geometry MOSFETs. In fact this equation assumes that the bulk depletion charge is only due to the electric field created by the gate voltage, while the depletion charge near n^+ source and drain region is actually induced by p-n junction band bending. Therefore, the amount of bulk charge the gate voltage supports is overestimated, leading to a larger V_{th} than the actual value. The electric flux lines generated by the charge on the MOS capacitor gate electrode terminate on the induced mobile carriers in the depletion region just under the gate. For short-channel MOSFETs, on the other hand, some of the field lines originating from the source and the drain electrodes terminate on charges in the channel region. Thus, less gate voltage is required to cause inversion. The shift in threshold voltage due to short channel effects can be given as

$$\Delta V_{T(short\ channel)} = -\frac{qNx_{dT}}{C_{ox}}\left[\frac{r_j}{L}\sqrt{1+\frac{2x_{dT}}{r_j}} - 1\right] \quad (4)$$

where x_{dT} denotes the lateral space charge width and r_j is the diffused junction.

At the same time, as the channel width is reduced, the narrow width effect can be expressed as

$$\Delta V_{T(narrow\ width)} = \frac{qNx_{dT}}{C_{ox}}\left[\frac{\xi x_{dT}}{W}\right] \quad (5)$$

where ξ denotes the shape of the fringe depletion region. So, considering the short channel and narrow width effect the modified threshold voltage can be expressed as

$$V_{TO} = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_{Si} q N_A (2\phi_F)}}{C_{ox}} - \frac{qNx_{dT}}{C_{ox}}\left[\left(\frac{r_j}{L}\sqrt{1+\frac{2x_{dT}}{r_j}}-1\right)-\left(\frac{\xi x_{dT}}{W}\right)\right] \quad (6)$$

The drain current as a function of threshold voltage and channel length and width can be expressed as

$$I_{d(lin)} = \mu_n C_{ox}\frac{W}{L}\left[(V_{gs}-V_{th})V_{ds} - \frac{V_{ds}^2}{2}\right] \quad (7)$$

and,

$$I_{d(sat)} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2 \quad (8)$$

This model describes the n-MOS device characteristics in terms of threshold voltage and channel length.

Results and Discussion

From the derived mathematical model it is clear that threshold voltage and channel length have certain effects on drain current. The typical value of threshold voltage for n-MOS transistor is 0.73V. To observe the effect of threshold voltage and channel length on drain current (at Temp = Tnom) the threshold voltage of transistor M2 is reduced from 0.73V to 0.5V (at $V_{bs} = 0$) and the simulation is performed for both long channel (L=20μm and W=200μm) and short channel (L=0.8μm and W=10μm) n-MOS using LTSPICE. The simulation data is then plotted and characterized using MatLab. The simulation model and I_d-V_{ds} characteristics curves for short channel and long channel MOSFET are shown in Fig. 2 and Fig. 3 respectively.

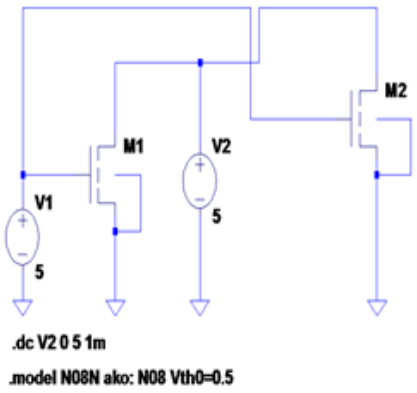

Fig. 2(a): Short channel n-MOS with L=0.8µm and W=10µm

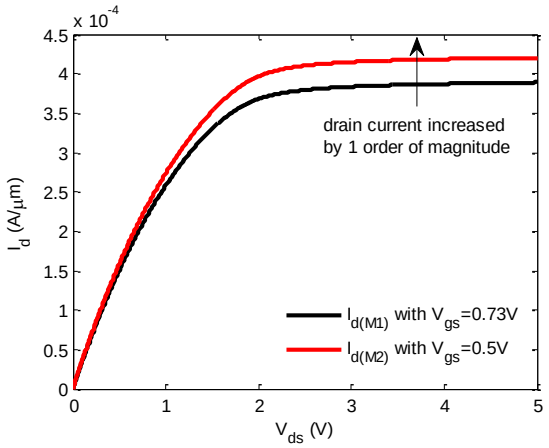

Fig. 2(b): I_d-V_{ds} characteristics curves showing the effect of short channel on drain current with reduced V_{th}. The drain current increased by 1 order of magnitude.

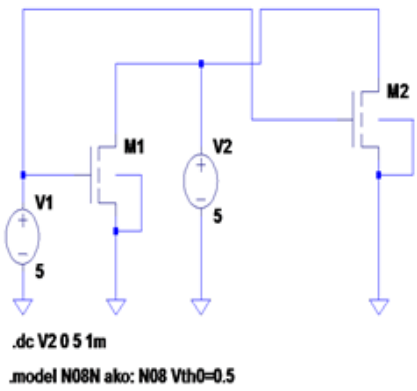

Fig. 3(a): Long channel n-MOS with L=20µm and W=200µm

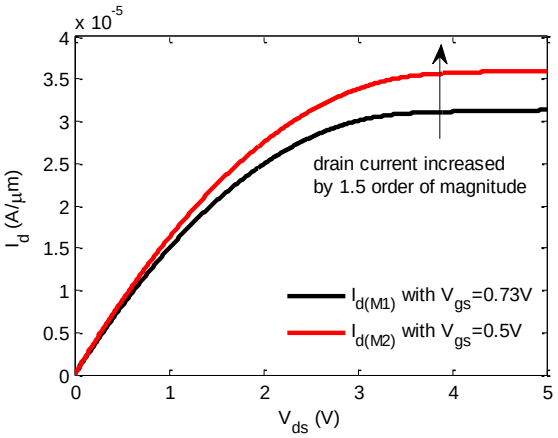

Fig. 3(b): I_d-V_{ds} characteristics curves showing the effect of Long channel on drain current with reduced V_{th}. The drain current increased by 1.5 orders of magnitude.

Form the above figures; it is evident that drain current increases for both short channel and long channel MOSFETs as the threshold voltage decreases. It is seen, the drain current per µm is more for short channel device but it increases more for long channel operation with the reduction of threshold voltage. Also for short channel n-MOS the curve is nearly aligned with horizontal than long channel n-MOS. It is called channel length modulation.

To illustrate the effect of short channel on threshold voltage two n-MOS transistors of model N08 are connected together as shown in Fig. 4(a). The devices are simulated and I_d-V_{gs} characteristics curves are obtained as

shown in Fig. 4(b), to observe the behavior of the threshold voltage and drain current at different geometry. Here, the length and width for M1 n-MOS of L=W=5.0µm and M2 n-MOS of L=W=0.5µm are considered where all other parameters are kept same.

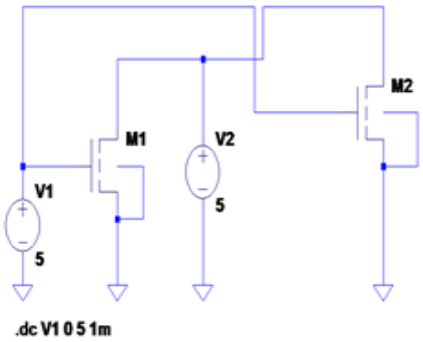

Fig. 4(a): Short channel n-MOS with L=W=5.0µm (M1) and L=W=0.5µm (M2)

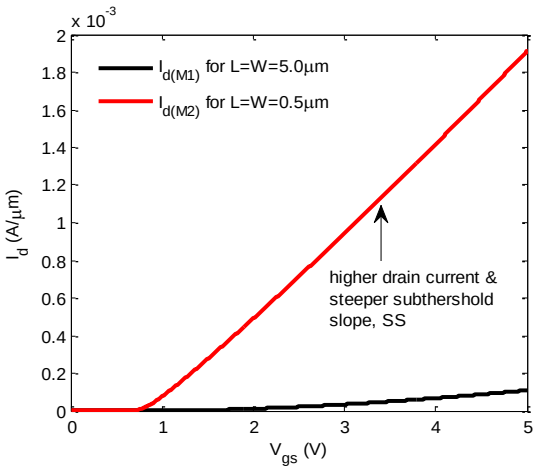

Fig. 4(b): I_d-V_{gs} characteristics curves showing the effect of short channel on V_{th} and drain current

It shows, device with smaller geometry have higher drain current at the same gate-to-source voltage; hence short channel device has lower threshold voltage.

Conclusion

This paper gives I_d-V_{ds} and I_d-V_{gs} characterization of Silicon n-MOSFET at room temperature by showing the effects of threshold voltage and channel length on drain current and investigating the short channel effect on threshold voltage. The simulation results obtained in this work are compatible with analytical model of short channel Si n-MOS which helps to characterize subthreshold behavior and device scaling. The further research can be done for III-V n-MOSFETs.

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