MICROPROCESSOR SYSTEM FOR VISUAL BAKED PRODUCTS CONTROL

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Abstract

The paper reports an authentic solution of a microprocessor system for visual control of baked products via Internet. The author suggests a structure of the microprocessor system. The microprocessor system was realized based on modern digital media processor TMS320DM6437. The descriptions of main elements are made. Operating principle of the microprocessor system is explained. An algorithm diagram on microprocessor control of baked goods is synthesized. Processing execution time for different resolution images is tested. An analysis of proposed microprocessor system is made.

Keywords: Microprocessor system, baked products, control

Introduction

Modern industrial requirements for baked products quality need visual control to be continuous with the possibility of traceability and recording of the process via the Internet. Modern microprocessor systems based on digital signal processors (**DSP**) provide an opportunity to objectively monitor the quality of baked goods. There are various methods for determining the quality of the food. In recent years as promising methods for objective assessment and visual control systems are established computer vision systems with integrated express estimation algorithms based on shape and color of processed foods (Sun, 2012). European standards for baked products for consumption require the implementation of express diagnostic systems for grading. There is a constant need for developing new systems ensure the high quality of food (Hui and Corke, 2008). In Europe, special attention is given to new developments allowing construction of advanced mobile autonomous systems using online grading based on opportunities of global networking monitoring via the Internet. The aim of this paper is to present a novel microprocessor system for visual baked products control based on modern digital media processor TMS320DM6437. Some basic algorithms are developed for system performance tests, because we know

that digital signal microprocessor are useless without software (Qureshi, 2005).

Design diagram and operating principle

Requirements to parameters of system for visual control of baked products are:

- baked product have to capture with speed 30 frame per seconds (fps);
- resolution of capture image have to be 720x480 pixel;
- embedded color image processing in the microprocessor system for baking control;
- local video monitoring via LCD display;
- Ethernet connection to the Internet;
- image compression for high speed networking transmission;
- low consummation below 10 W;
- portability for mobile quality system.

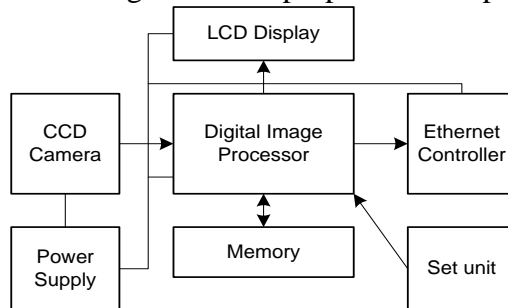Fig. 1 shows the block diagram of the proposed microprocessor system.

Figure 1. Block diagram of the system

The microprocessor system in Fig.1 consists of:

- power supply which provides safe continuous voltage of 5 V for the operation of the system;
- digital image processor for video and image processing to control the all elements and provide an opportunity to objectively monitor the quality of baked goods;
- CCD camera with standard output signals for capturing of baked product color images;
- set unit for selecting the operation mode;
- memory for program and images store.
- Ethernet controller for realization of internet connection.

The author designs a full working microprocessor system and implements algorithms for visual baked products control. The author uses a new kind of digital media processor (DMP) for his proposed microprocessor system, because modern DMPs are flexible and suitable to extremely

complex math intensive video tasks and have integrated network interface. The presented system is suitable for online visual monitoring control for all types of baked products by conveyer moving. Some basic algorithms are developed for system performance tests.

Design of the microprocessor system

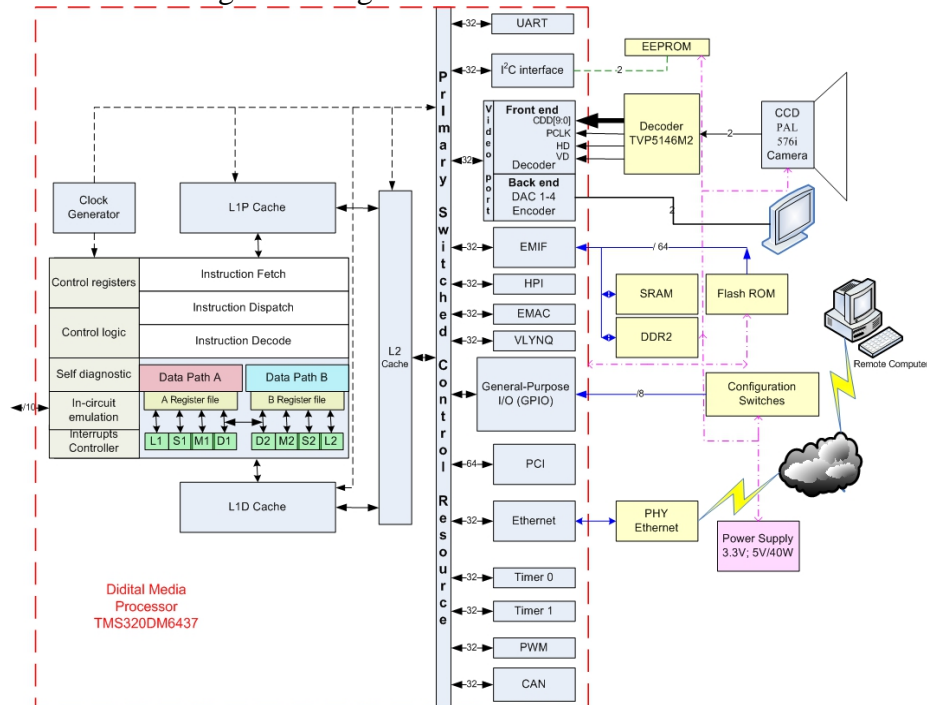Diagram of the designed microprocessor system for visual baked products control is given in Fig.2.

Figure 2. Diagram of the microprocessor system

The author uses the high performance **DMP** chip TMS320DM6437 of Texas Instrument (**TI**) as a core, design and realizes a whole hardware subsystem. The TMS320DM6437 offers cost-effective solutions to high-performance **DSP** programming challenges with up to 5600 MIPS at a clock rate of 700 MHz. The core processor has 64 general-purpose registers of 32-bit word length, two multipliers for a 32-bit result and six arithmetic logic units (ALUs). The DM6437 core uses a two-level cache-based architecture. The Level 1 program memory/cache (**L1P**) consists of a 256K-bit memory space that can be configured as mapped memory or direct mapped cache, and the Level 1 data (**L1D**) consists of a 640K-bit memory space, 384K-bit of which is mapped memory and 256K-bit of which can be configured as mapped memory or 2-way set-associative cache. The Level 2 memory/cache (**L2**) consists of a 1M-bit memory space that is shared between program and

data space. **L2** memory can be configured as mapped memory, cache, or combinations of the two. The DM6437 device includes a Video Processing Subsystem (**VPSS**) with two configurable video/imaging peripherals: one Video Processing Front-End (**VPFE**) input used for video capture, one Video Processing Back-End (**VPBE**) output. The peripheral set includes: two configurable video ports; a 10/100 Mb/s Ethernet MAC (**EMAC**) with a management data input/output (**MDIO**) module; a 4-bit transmit, 4-bit receive VLYNQ interface; an inter-integrated circuit (**I^{2}C**) Bus interface; two multichannel buffered serial ports (**McBSPs**); a multichannel audio serial port (**McASP0**) with 4 serializers; two 64-bit general-purpose timers each configurable as two independent 32-bit timers; one 64-bit watchdog timer; a user-configurable 16-bit host-port interface (**HPI**); up to 111-pins of general-purpose input/output (**GPIO**) with programmable interrupt/event generation modes, multiplexed with other peripherals; two universal asynchronous receiver/transmitters (**UART**s) with hardware handshaking support on one **UART**; 3 pulse width modulator (**PWM**) peripherals; one high-end controller area network (**CAN**) controller; one peripheral component interconnect (**PCI**); and two glueless external memory interfaces: an asynchronous external memory interface (**EMIFA**) for slower memories/peripherals, and a higher speed synchronous memory interface for DDR2 (Texas Instruments Incorporated, 2008). The microprocessor system has a large byte addressable address space. Program code and data can be placed anywhere in the unified address space. The given system incorporates a 64 bit wide external memory interface. Addresses are always 32-bits wide. By default, the internal memory sets at the beginning of the address space. The EMIF (External Memory Interface) used to serve external memory. The external memories of system consist of a 128 Mbytes of DDR2 SDRAM, 16 Mbytes of non-volatile Flash memory and 2 Mbytes SRAM. DDR2 is used for program, data, and video storage. Memory refresh for DDR2 is handled automatically by the TMS320DM6437. The microprocessor system has a two configuration switches to control the operational state of the processor. The microprocessor system incorporates an I^{2}C EEPROM with capacity of 1MB for booting purpose. The TMS320DM6437 has an internal PLL which can multiply the input clock to generate the internal clock.

Decoder TVP5146M2 is used to decode composite video input into the VPFE of the TMS320DM6437.

The image color camera SONY SUPER HAD II CCD with composite video output was chosen as input device to capture continuous video frames progressively with speed 30 fps. The camera works according NTSC 480i video signal with resolution 720x480 pixels. The external connection to the Internet is via PHY Ethernet interface Micrel KS8001L.

The 10/100 Mbit interface is isolated and brought out to a RJ-45 standard Ethernet connector. The PHY directly interfaces to the **DMP**.

Software Structure

The input images are loaded into the **DMP** by decoder TVP5146M2 with mode YUV4:2:2. An algorithm for visual control of baked products is shown in Fig.3.
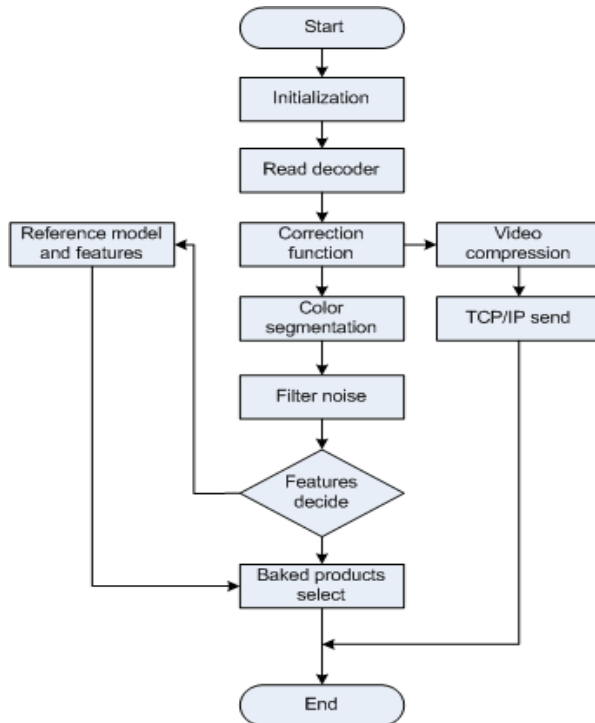

Figure 3. An algorithmic structure for visual control of baked products

Firstly, the computer system is initialized hardware components. Then it read first frame from decoder and corrected image according light conditions. The corrected frame is compressed by H.264 standard for TCP/IP transmission. Color segmentation is made by Mahalanobis distance calculation according the equation:

squared_distance(Cb;Cr) = (x-m)′ x inv C(x-m),

(1)

where: m is mean, C is covariance matrix and x = [Cb;Cr].′The result is compared with the threshold value, enabling detection of the baked product color. The result of the segmentation algorithm is a binary image (Gonzalez and Woods, 2011), whose pixels with values equal to one indicate location of the baked color in the input image. This binary baked map is compared with the original image. The filtration is made by median filtering. Median filter are removing outlier type noises. The computation of the

median filter starts at ordering those n pixels defined by the filter mask, in order from minimum to maximum value of the pixels as given in equation below:

$$F_0 \leq F_1 \leq \ldots \ldots \leq F_{n-1}, \tag{2}$$

where F_0 denotes the minimum and F_{n-1} is the maximum of all the pixels in the filter calculation. The output of the median filter is median of these value and is given by

$$F_{med} = \begin{cases} \dfrac{F_{n/2} + F_{n/2-1}}{2} & for\ n\ even \\[2mm] F_{n/2} & for\ n\ odd \end{cases} \tag{3}$$

On the detection of regions of baked products is taken the Sobel operation on candidate region to find out the features of the product. Sobel operator is an operator used mainly in image processing for edge detection. Sobel operator is a discrete difference operator and defined in the following formulas:

$$G_x = \begin{vmatrix} -1 & 0 & 1 \\ -2 & 0 & 2 \\ -1 & 0 & 1 \end{vmatrix} * A \tag{4}$$

$$G_y = \begin{vmatrix} 1 & 2 & 1 \\ 0 & 0 & 0 \\ -1 & -2 & -1 \end{vmatrix} * A \tag{5}$$

$$G = \sqrt{G_x^2 + G_y^2} \tag{6}$$

Where Gx, Gy and G are the x- component matrix, y –component matrix and the magnitude of gradient of image matrix A respectively.

Compression is the type of H.264 and was performed taking into consideration of the standard (ITU, 2014). Programming of the system is made by set block commands. Same block examples are shown in Fig. 4.
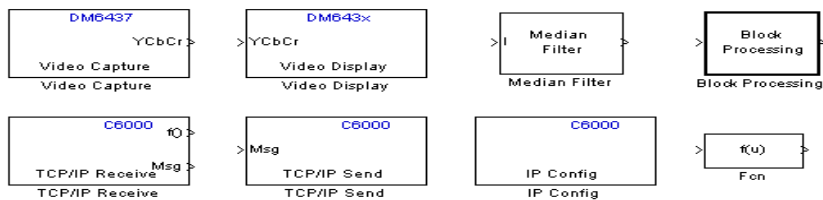

Figure 4. Block command for programming

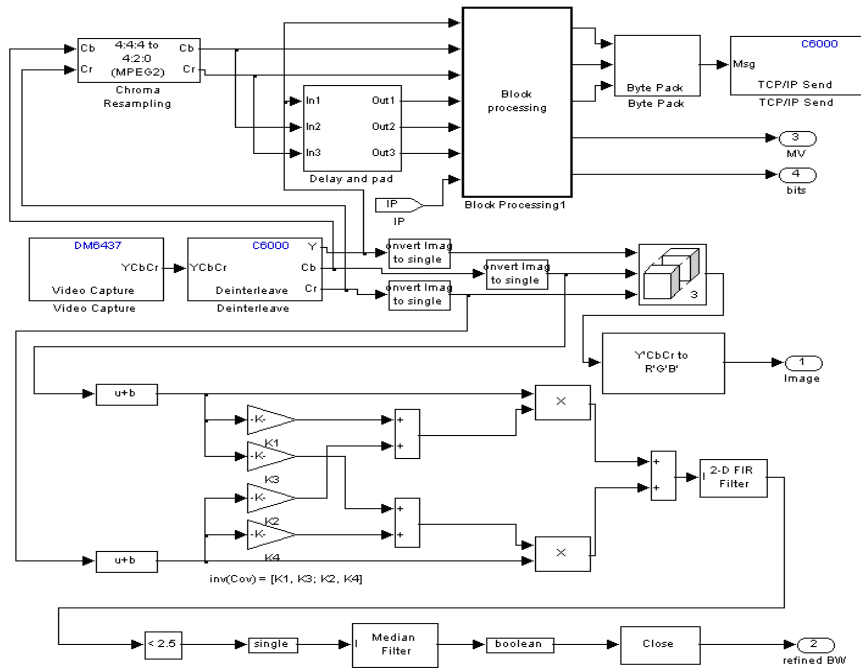A sample program code is shown in Fig. 5.

Figure 5. A sample program code

The size of programming code depends on program realization of algorithms.

System test

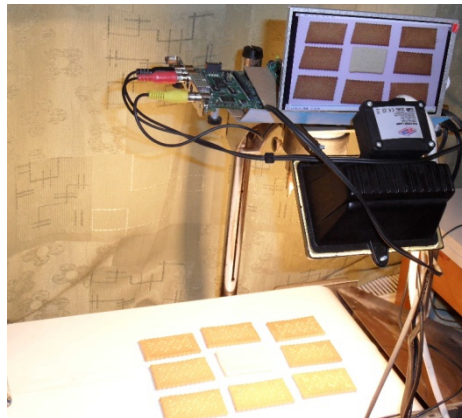The proposed microprocessor system is shown in Fig. 6

Figure 6. The microprocessor system for visual control of baked products

The development test of the microprocessor system was made with biscuits. The capture speed is constant 30 fps. The maximal size of

processing image is 720x420 pixels and minimal size of processing image is 120x70 pixels. The algorithms are realized by set blocks. Features are calculated by Sobel operator. Table 1 shows the results of processing execution time for each of the algorithms realized in the microprocessor system.

Table 1. Values of processing time in proposed microprocessor system

Algorithms	Execution time [s]		
	for image resolution 720x420	for image resolution 180x105	for image resolution 120x70
Initialization	$5.87*10^{-6}$	$5.87*10^{-6}$	$5.87*10^{-6}$
Color segmentation	5.2	0.25	0.07
Median filtering 3*3	0.008	0.0005	0.0003
Feature decide	6.1	0.3	0.08

For tests, the line bandwidth of server-side of the microprocessor system and packet generating of the microprocessor system is fixed at 100M bps, and the client-side line bandwidth of computer is fixed at 10M bps, The real test for different packets show that network transmission bandwidth is only 1.3Mbps for block set H.264 realization. The H.264 algorithm reduces frames per second to meet the situation of only 1.5Mbps bandwidth and the picture quality is reduced.

The actual power consumption in this experiment with proposed microprocessor system based on TMS320DM6437 is 6.4 W. The total maximum power consumption of all components of the microprocessor system is less than 8 W, according to component manufacturers

Conclusion

This paper discusses a microprocessor based design of a novel system for visual control of baked products via Internet using the modern digital media processor TMS320DM6437.The operating principles and construction of the microprocessor system have been explained. The cost of the proposed device is around EUR 200. The performance test result shows that this microprocessor system has total processing time depends on size of processing image. For image with resolution 120x70 pixel total execution time is under 0.151 seconds. The proposed microprocessor system based on high performance video signal processor TMS320DM6437 has small size, power consummation under 8 W and can use as mobile quality evaluation platform on production lines. Other advantage of the proposed system is opportunities for expansion and network connection via Ethernet, as each microprocessor system have individual MAC and IP addresses. An innovative microprocessor system for baked products quality evaluation is shown in this paper.

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