SMART AUDIO AMPLIFIER

Josue Zarate V,
Enrique Muñoz C,
Ruben Diaz C.
School of Mechanical and Electrical Engineering
University San Luis Gonzaga, Peru

Abstract

This project focuses on the control of audio power amplifiers. Is the development and implementation of a system of controlled cooling and optimizing the power consumption and temperature generated, using an advanced control algorithm. The approach is based on the configurations of integrated circuits (IC) audio amplifiers allowing us to obtain data energy consumption and parameters of temperature gradient, generally with the required parameters will be processed by a microcontroller (uC) to pass to run programmed by a control algorithm(PID) instructions. The design of the electronic circuit is composed of passive and active electronic devices essentially controlled by protocol (I2C / TWI), Class-T Digital Audio Amplifier, sensors, microcontrollers working on master and slave protocol using UART mode. Configurations and analysis by module (ADC), including a turning on system and automatic shutdown and peripherals, the frequency at which works is 20Hz to 20kHz with 75dB decibel maximum. Finally both analysis and theoretical control simulation showed that the use of a good control configuration based on energy regulation and switching amplifiers allows the temperature was controlling with excellent accuracy and reduces wear on stage of electronic circuit.

Keywords: IC, PID, UART, ADC

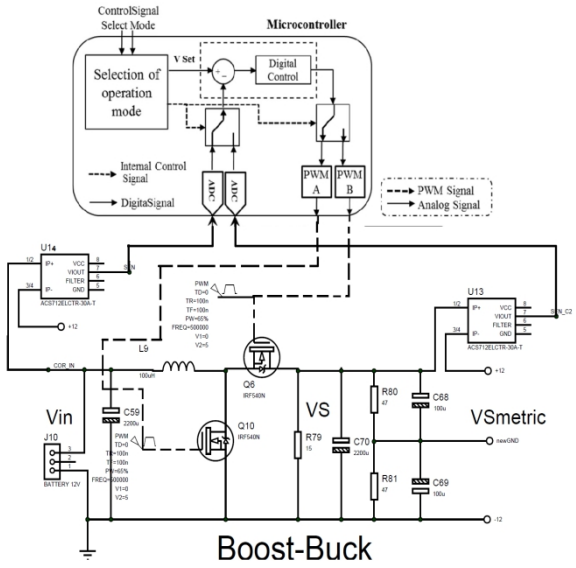
Introduction

Currently in the audio amplifiers be perceived the need an efficient moderate sound control and good cooling system, either in various configurations amplification circuits. Often used this ventilation system. Focused on generating gain and amplifying the incoming signal to be then sent to the output load, thereby leaving out the cooling control system, and especially the required consumption of each stage. Thereby causing severe problems in integrated circuit devices and power because the temperature

generated by them. Therefore it is possible to control said temperature generated and directly proportional current consumption. Thus, it becomes absolutely necessary to have an automated system that monitors each stage, from the detection to amplification stage. Using data obtained mainly from the sensors and integrated circuits. It is therefore necessary to be able to identify parameters of possible short circuits and wrong power settings, these walls will be able to isolate the supply of each stage. Therefore, to accomplish this task control and identification is essential to have an algorithm that this widespread with each stage of the design is done through a hardware that has the necessary pattern recognition algorithms. Also, In other words this project focuses on minimizing consumption and optimize control by providing an alternative solution for easy access.

Methodolog

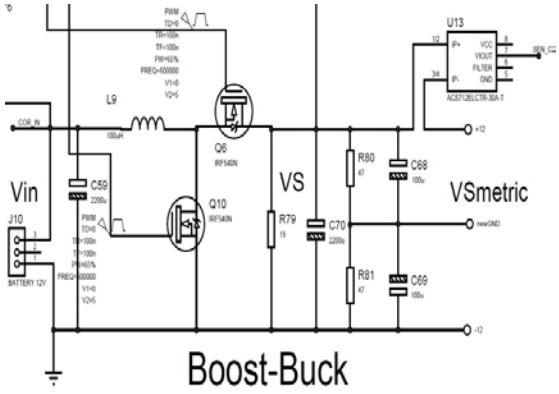
The realization of this project involved the development of different stages from incoming detection and sensor signals to implementation of pattern recognition algorithm in the microcontroller, with their respective tests and as a result the power amplification. It should be clarified that for the development of this project, some steps were implemented in Software Matlab / Simulink, while others using the C ++ Programming Language. As for the simulation was performed by proteus (Isis) and finally Tera term. The Matlab / Simulink was used because this software offers versatility for programming and also a practical management for implementation and training power circuits. The Proteus was used to perform the simulation of our ele.ctronic circuit design, this software performs simulations 300MHz to this simulation with the frequency set with real time simulation. The first step is the configuration and gain power for the entire electronic circuit, the second stage was responsible for the pre-amplified signal, then the third stage dealt with the implementation of the algorithm in the microcontroller, and the last is devoted itself power amplification. It is clear that each has a purpose estapa that interacts with the microcontroller via sensors and ADC ports that are responsible for obtaining the parameters required by the algorithm. In this way we can also implement a communication and interaction with the computer through the serial port. The following outlines each of the steps implemented for the development of this development Project:



1.-Power: configuration and control. It is known that in audio stages is counted as the preamplifier, that is required for positive and negative intentions worth highlighting the need for symmetric source. Therefore. Speaking about the power configuration is referable to use an elevator retention. That in this section discuss it. Thus, to generate an appropriate retention for stage, it is appropriate input power as prime 12V, sombre this intention is implemented in hardware a DC / DC converter to take care of delivering the power and intention necessary for the pre-amplification circuit, also the amplification circuit average power, it a 5 volt supply is regulated by the regulator built 7805, it will be necessary to power the control circuit.

1.1.-Boost-Buck converter in closed loop

Figure shows the bidirectional boost-buck converter used to increase the



voltage from input Vin, to the DC bus voltage level VS. Such a converter also supports the inverse power flow in buck operation mode from VS (DC

bus or regenerative load) to Vin (auxiliary storage device). The MOSFET used in the converter was a N-channel IRF540N from International Rectifier. It is noted that Q10 and Q6 MOSFETs activation are complementary to avoid fuel cell short-circuits: in boost mode the Q10 MOSFET is the independent one and Q6 is activated by a complementary signal, while in buck mode the Q6 MOSFET is the independent one and Q10 is activated by a complementary signal. The bidirectional converter is controlled by means of a 500 kHz and 65% PWM a(Pulse Width Modulation), and its control structure is depicted in **Figure,** depending on the required power flow direction, the microcontroller drives Q10 and Q6 MOSFETs by means of a PID controller. In addition, the converter passive elements were calculated to fulfill the fuel cell small current ripple requirement considering a DC bus voltage equal to 24 V with 3A, and fuel cell and auxiliary storage voltages within the range [5,5-11,5] V. The nominal power of the converter is then 50 W, and its inductor design ensures a continuous conduction mode (CCM) for the adopted operating conditions. The converter parameters are: L9 = 100 µH, C59 = 2200 µF, C70 = 2200 µF and R79 = 15 Ω.

The converter was controlled by using an ATmega32 microcontroller (Atmel Corporation), where the input and output port voltages are measured to calculate the control signal as in (1),(2). In such equations e represents the error signal used to process the PID controller, Vref represents the desired voltage, and Vme represents the measured voltage: DC bus or load voltage for the boost mode, and auxiliary storage or fuel cell voltage for the buck mode. The error signal is calculated in each duty cycle period, as well as the control command that defines the converter duty cycle generated by the PID structure given in (2), where Kp is the proportional constant, Ki the integral constant and Kd the derivative constant.

$$\boldsymbol{e = V_{ref} - V_{me}} \qquad \mathbf{1})$$

$$\boldsymbol{C(t) = Kp * e(t) + Ki * \int_0^t e(t) * dt + Kd * \frac{de(t)}{dt}} \qquad \mathbf{2})$$

Since the ATmega32 microcontroller process only digital equations, the analogue controller given in (2) has been digitalized in difference equations as given in (3), where Ti = 1/Ki represents the integral time constant, Td = Kd the derivative time constant, and Ts the sampling time.

$$C(n) = Kp * e(n) + \frac{Ts}{Ti} * \sum_0^N e(n) + \frac{Td}{Ts} * [e(n) - e(n-1)] \qquad (3)$$

The controller parameters were designed by means of the root-locus placement technique by using the small signal models of both boost and buck circuits. In this way, the small-signal model of the boost converter is:

$$\begin{bmatrix}\hat{x}_1(s)\\ \hat{x}_2(s)\end{bmatrix}=\frac{\begin{bmatrix}s+\frac{1}{RoC2} & -\frac{(1-D)}{L}\\ \frac{(1-D)}{C2} & s\end{bmatrix}}{s^2+\frac{s}{RoC2}+\frac{(1-D)^2}{LC2}}*\left[\begin{bmatrix}\frac{1}{L} & 0\\ 0 & \frac{1}{C2}\end{bmatrix}*\begin{bmatrix}\hat{u}_1(s)\\ \hat{u}_2(s)\end{bmatrix}+\begin{bmatrix}\frac{X_{20}}{L}\\ -\frac{X_{10}}{C2}\end{bmatrix}*\left[\hat{d}(s)\right]\right] \quad (4)$$

Where $x1$ represents the inductor current, $x2$ the $C2$ capacitor voltage, $u1$ the input voltage (main or auxiliary power source), $u2$ models the load perturbations, d and D represents the converter small-signal and steady-state duty cycle values, respectively. In such a model the capital letters denote steady-state values, and the small-signal single input-single output transfer function between the output voltage $x2\hat{}$ and the duty cycle $d\hat{}$ is:

$$\frac{\hat{x}_2(s)}{\hat{d}(s)}=\frac{\frac{(1-D)*X_{20}}{LC2}-s*\frac{X_{10}}{C2}}{s^2+\frac{s}{RoC2}+\frac{(1-D)^2}{LC2}} \quad (5)$$

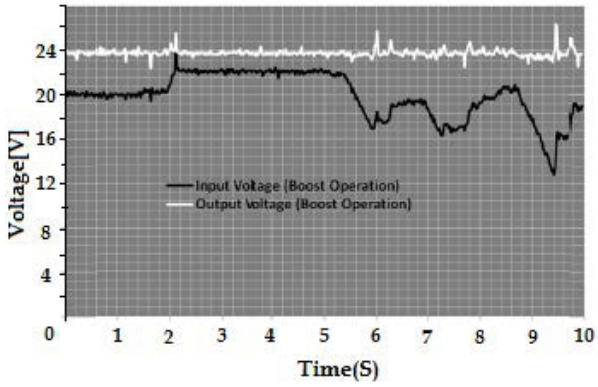
The controller designed for this operating mode has the following parameters: $Kp = 0{,}3$; $Ki = 0{,}001$; $Kd = 0$; this with a $Ts = 2ms$. In a similar way, the small-signal model of the buck coverter is given by (6), where $x1$ represents the inductor current, $x2$ the $C1$ capacitor voltage, and u1 the input voltage. Equation 7 gives the small-signal single input-single output transfer function between the output voltage $x2\hat{}$ and the duty $d\hat{}$ cycle used to design the following controller parameters: $Kp = 0{,}25$; $Ki = 0{,}0001$; $Kd = 0$; $Ts = 2\,ms$.

$$\begin{bmatrix}\hat{x}_1(s)\\ \hat{x}_2(s)\end{bmatrix}=\frac{\begin{bmatrix}s+\frac{1}{RoC1} & -\frac{1}{L}\\ \frac{1}{C1} & s\end{bmatrix}}{s^2+\frac{s}{RoC1}+\frac{1}{LC1}}*\left[\begin{bmatrix}\frac{D}{L}\\ 0\end{bmatrix}*\left[\hat{u}_1(s)\right]+\begin{bmatrix}\frac{U_{10}}{L}\\ 0\end{bmatrix}*\left[\hat{d}(s)\right]\right] \quad (6)$$

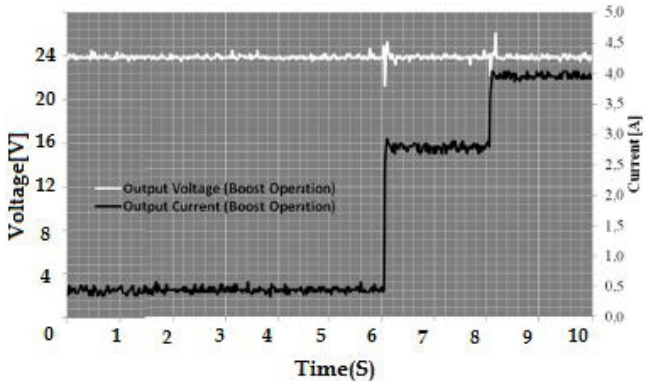
$$\frac{\hat{x}_2(s)}{\hat{d}(s)}=\frac{\frac{U_{10}}{LC1}}{s^2+\frac{s}{RoC1}+\frac{1}{LC1}} \quad (7)$$

The closed loop bidirectional DC/DC converter has been experimentally tested in both boost and buck modes. The boost mode was evaluated by defining a regulated 24 VDC bus voltage, where perturbations on the DC bus current and power source voltage, i.e. fuel cell or auxiliary

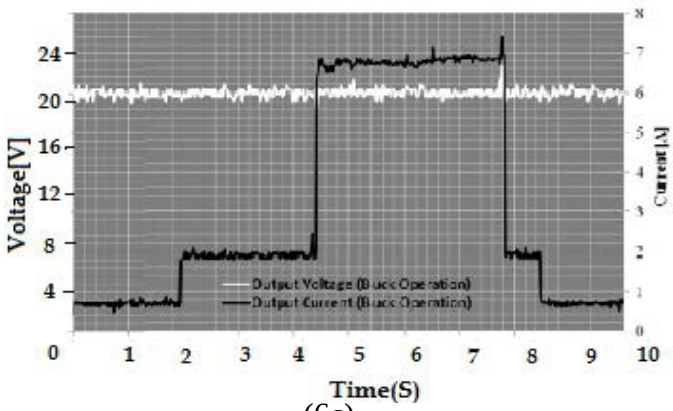
storage device, were applied. The test defines a DC bus impedance equal to 15Ω , and low frequency variations between 11,5 V and 5,5 V were applied to the input port voltage, which are typical on fuel cells and high capacitive storage devices. In such conditions the system behavior is satisfactory as reported in figure 6a, where the DC bus voltage is accurately regulated in presence of the input voltage perturbations. An additional experiment was performed in boost mode by defining a constant input port voltage equal to 9V and applying perturbations to the DC bus impedance: it starts at 15Ω, then it is decreased to 4,52Ω, and finally it is further reduced to 3,11Ω. This test evaluates the performance of the converter and its controller in load perturbations. The experimental results are depicted in figure 6b, where it is observed the satisfactory response of the closed loop converter in the DC bus voltage regulation.



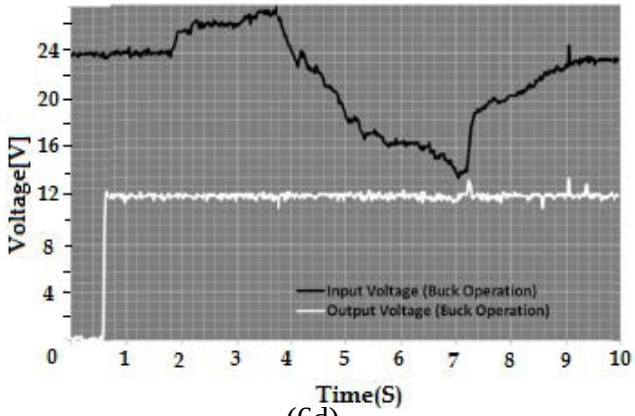
(6a)



(6b)



(6c)



(6d)

Figure 6

Experimental dynamic response of the closed loop bidirectional converter: a) boost mode with input voltage transient; b) boost mode with load current transient; c) buck mode with input voltage transient; d) buck mode with load current transient. Finally, it is noted that in the boost operating Mode the steady-state voltage error is lower than 0,8 %, while in buck mode it is lower than 0,3 %. Such experimental results illustrate the accurate regulation of the device.

2. Signal Preamplifier. Preamplifier circuit is developed based on the use of high-speed operational amplifiers and sensitivity, it should be noted that these characteristics is essential for audio signals. Since it will take as input a range of 10mV to 100mV, be necessary to design this circuit.

2.1.-Preamplifier Circuit with TL072**.** The JFET-input operational amplifiers in the TL072 with low input bias and offset currents and fast

slew rate. The low harmonic distortion and low noise make the TL072 series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip. The C-suffix devices are characterized for operation of High Input Impedance: JFET Input Stage and High Slew Rate.

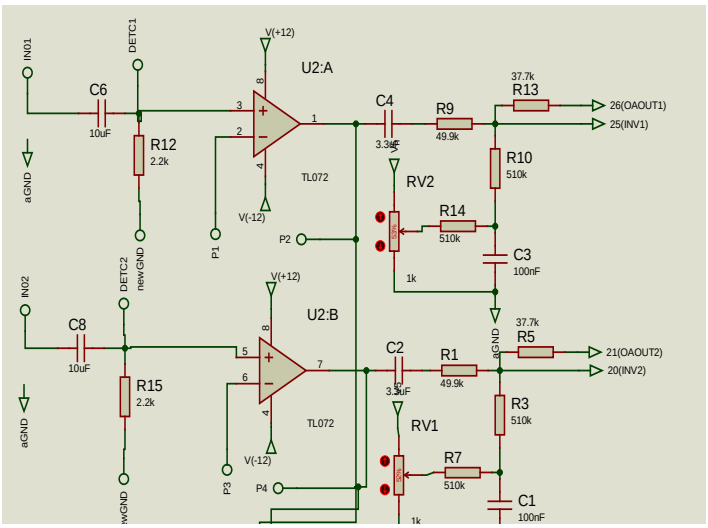
2.2.-Preamplifier Configurations. The preamp design a circuit is to optimize the signal enters and filter noise signals, the application aims to make profits will depend on how they are configured. In this case the TL072 was used in two types of mode settings, non-inverting amplifier and a follower amplifier.

2.2.1. Op-Amp Non-Inverting Amplier. Is indispensable to obtain as output the noninverting input signal, in turn there will be obtained a gain appropriate voltage to the power amplifier. The circuit has two digital potentiometers the AD5220BN100 that will be very useful to control gains control system as this will depend on the signals to be sent to the power circuit. The C6, C8 with R12, R15 perform the function filters the incoming signal characterized by a high impedance Z for frequencies below 10Hz.

$$F = 1 / (2\pi \; x \; C6 \; x \; R12)$$

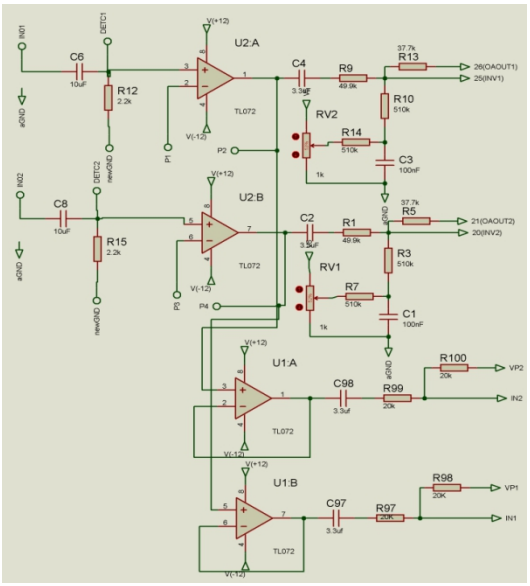
$$F = \frac{1}{2\pi \; x \; 10uf \; x \; 2.2} = 7 \; .234 \; Hz$$

C6=C8=10uf, R12=R15=2.2KΩ, F<10Hz



The gain depends on the Digipots, these are connected in the order [P2-P1] will be like a resistor (R2), [P1-newGND] be a resistor (R1). $\Delta V = 1 + R2 / R1$

$$Vo = \Delta V * Vin$$



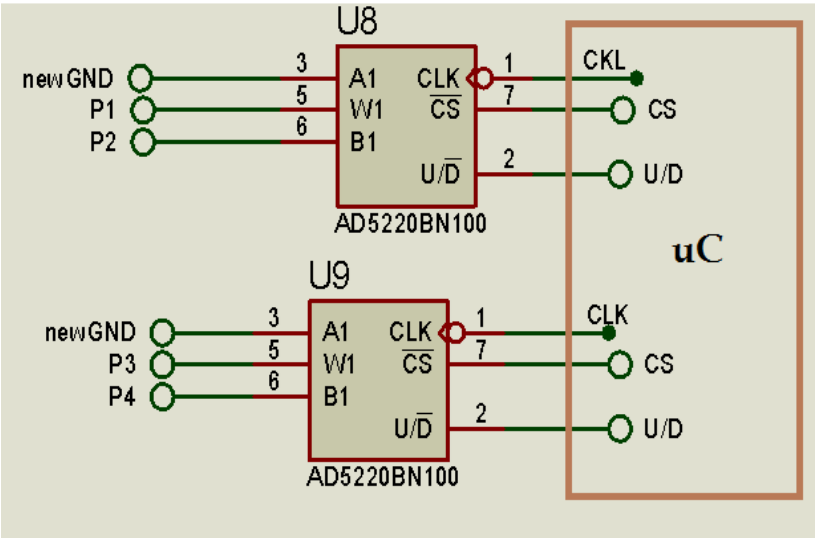
Digital potentiometers U8 = U9 = 100KΩ are configured by the microcontroller (ATmega32) and if the input is 50mV as the uC using the ADC reads the 50mV digitally, this led to act in uC, setting the two potentiometers are connected in parallel. Modifying and R1 = R2 = 93KΩ 7KΩ. As a result it will 714.29mV.

$$\Delta V = 1 + \frac{93K}{7K} = 14.2857$$

$$Vo = 14.2857\ x\ 50mV = 714.29mV$$

It should be noted that the non-inverting amplifier signal is sent to the power amplifier, which is 300W (TA3020).

2.2.2.-The follower amplifier. Was used to maintain the amplitude of the signal and the gain provided by the noninverting amplifier. That said have a gain equal to the .DELTA.V = 1 and Vo = Vin unit. In figure shows U1: A, U1: B amplifier configured as a follower. If the Vin = 714.29mV since it will result to Vo = 714.29mV. Clearly, the signal is sent to a follower amplifier average power is 10W (TA1101B).

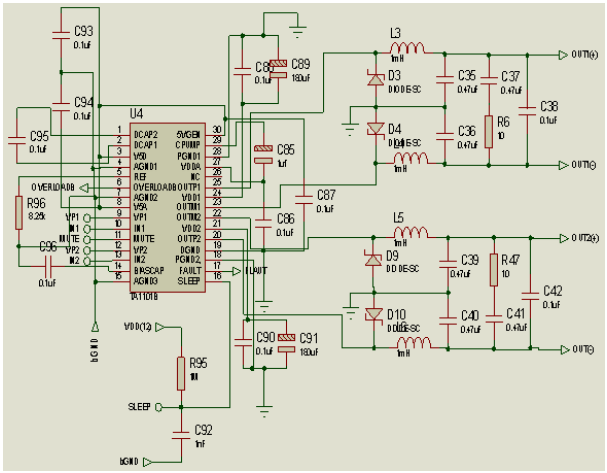


3. Power Amplifier Circuit. At this stage the circuit is designed based on class T amplifiers Both amplifiers offer the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers. In search of the proper and efficient amplifier, was reached to selecting two integrated audio amplifiers. Audio Integrated circuits are **TA1101B**, **TA3020**. These amplifiers are really optimal and efficient for those characterized.

- Fully integrated solution with FETs
- Class-T architecture
- Easier to design-in than Class-D
- Reduced system cost with no heat sink
- Dramatically improves efficiency versus class –AB
- Signal fidelity equal to high quality linear amplifiers
- Dynamic Range >= 102 Db

The TA1101B operates by generating a high frequency switching signal based on the audio input. This signal is sent through a low-pass filter (external to the Tripath amplifier) that recovers an amplified version of the audio input. The frequency of the switching pattern is spread spectrum and

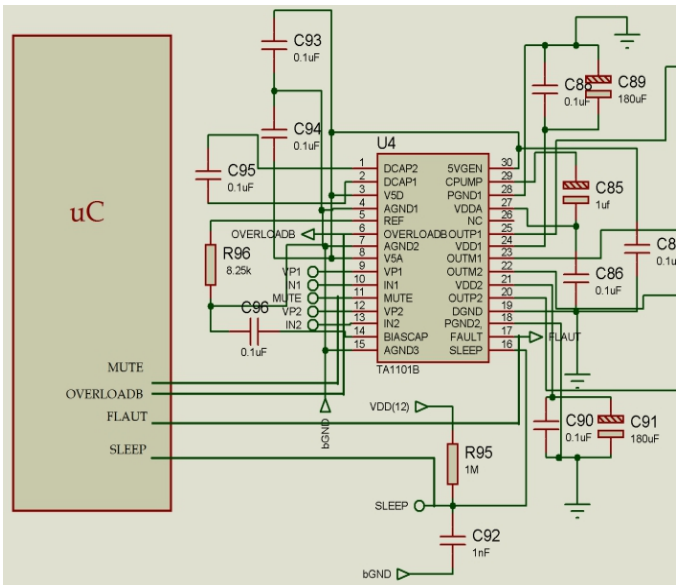
typically varies between 100kHz and 1.0MHz, which is well above the 20Hz–20kHz audio band. The pattern itself does not alter or distort the audio input signal but it does introduce some inaudible components. The design and configuration of CI TA1001B shown in the figure.



Where VI is the input signal level and VO is the differential output signal level across the speaker 9.18Watts of RMS potput power results from an 8.57V RMS signal acrros and 8Ω speaker load. If R100=R99 then 9.18W will ber achieved with 714.29mV of input signal.

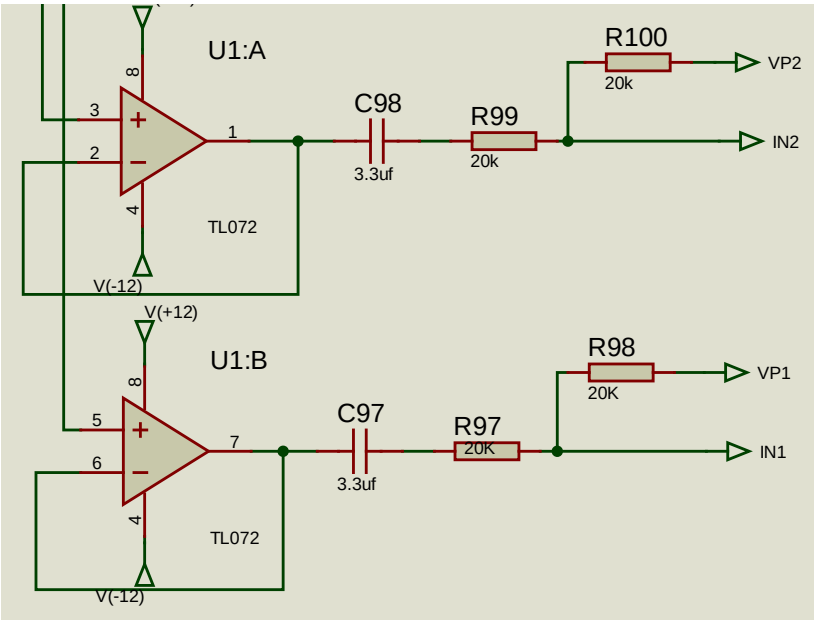
$$VO = 12 * 714.29mV = 8.57\, VVO = \sqrt{8 * 9.18} = 8.57V$$

18Watts of RMS output power results from an 8.57V RMSsignal across and 8Ω speaker load. If R100=R9



3.1.-10W Amplifier.For amplification reaches generate a power of 10W we resorted to implement integrated audio amplifier TA1101B. Besides supporting said as efficient as power and class AB, D apart from that requires only 12V supply. Physically has a small footprint, this makes prefect to save space

3.1.1.-Amplifier Gain. In the figure the pre-amplification circuit which is implemented is shown. We can say that VP2, N2, VP1, N1 are the pins belonging to the amplifier input TA1101B



The gain of the TA1101B is set by the ratio of two external resistors, $R99, R97$. and $R100, R98$, and is given by the following formulate:

$$\Delta V = \frac{VO}{VI} = 12 * \frac{R100}{R99} = 12 * \frac{20k}{20k} = 12$$

$$VO = 12 * 714.29mV = 8.57\, VVO = \sqrt{8 * 9.18} = 8.57V$$

3.1.2.-TA1101B interaction w/ATMEGA32 uC

The integrated is interacting through peripherals with OVERLOADB, Flaut, SLEEP, MUTE. While OUTP1, OUTP2 amplifier outputs are to be connected directly to two audio loads.

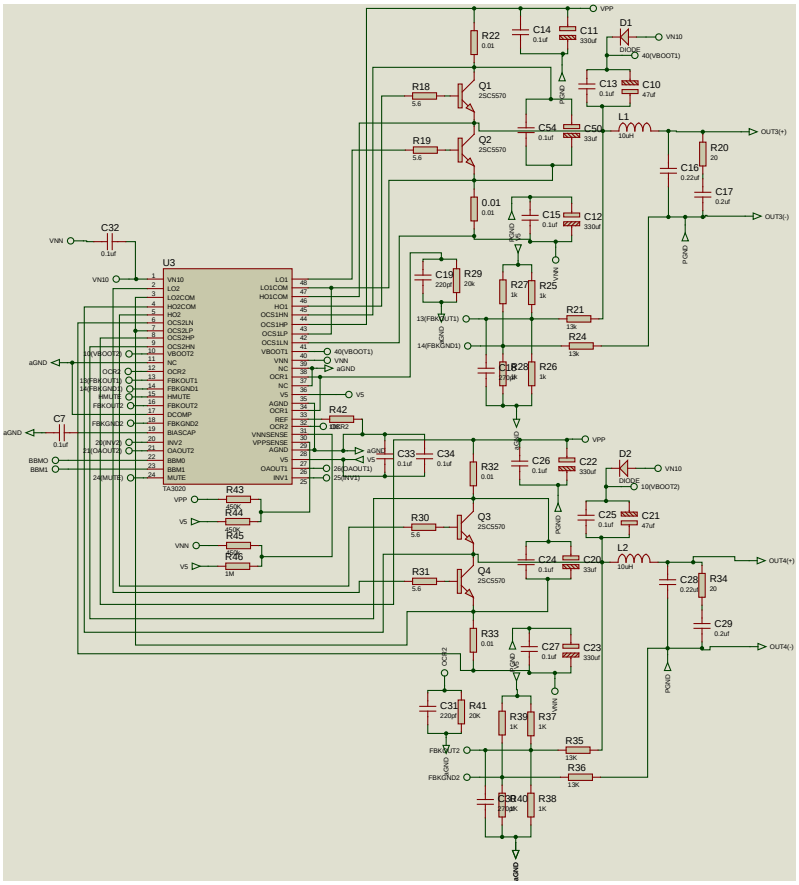
The OVERLOADB pin is a 5V logic output. When low, it indicates that the level of the input signal has overloaded the amplifier resulting in increased distortion at the output. The OVERLOADB signal is used to control a distortion indicator light.

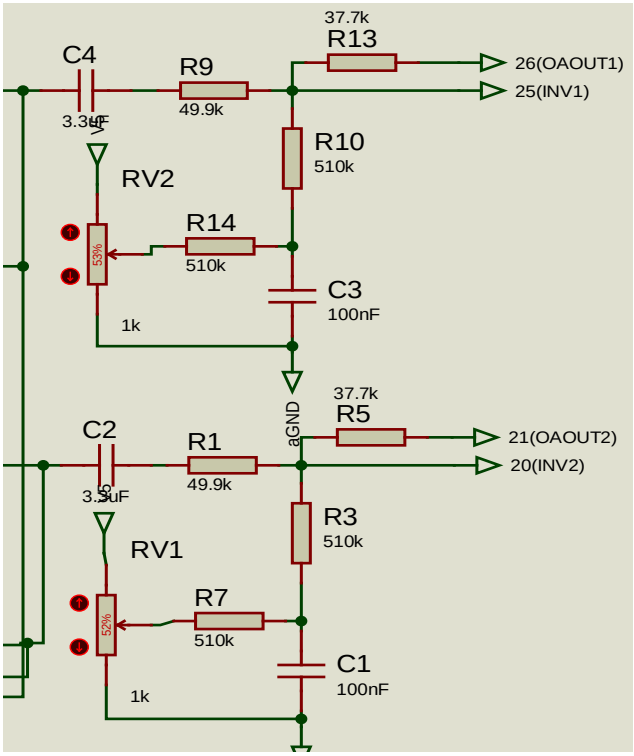
The FAULT pin is a 5V logic output that indicates various fault conditions within the device. These conditions include: low supply voltage, low charge pump voltage, low 5V regulator voltage, over current at any output, and junction temperature greater than approximately 155°C. All faults except overcurrent all reset upon removal of the condition.

The SLEEP pin is a 5V logic input that when pulled high (>3.5V) puts the part into a low quiescent current mode. This pin is internally clamped by a zener diode to approximately 6V. To disable SLEEP mode, the sleep pin should be grounded.

The MUTE pin When set to logic high, both amplifiers are muted and in idle mode. When low (grounded), both amplifiers are fully operational. If left floating, the device stays in the mute mode. Ground if not used.

3.2.-<u>300W Amplifier</u>**.** For obtain this powering is implemented with TA3020, is a stereo power amplifier. As the amplifier is TA1101B T class and is therefore much more efficient than any high power amplifier since this can generate more profit and achieve very high power greater than 1000W.



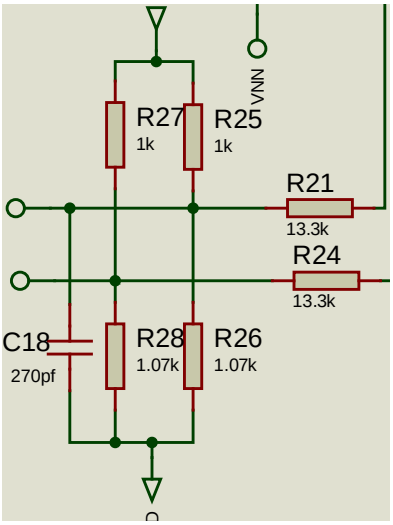


The audio input signal is fed to the processor internal to the TA3020, where a switching pattern is generated. The average idle (no input) switching frequency is approximately 700kHz. With an input signal, the pattern is spread spectrum and varies between approximately 200kHz and 1.5MHz depending on input signal level and frequency. Complementary copies of the switching pattern are level-shifted by the MOSFET drivers and output from the TA3020 where they drive the gates (HO1 and LO1) of external power MOSFETs that are connected as a half bridge. The output of the half bridge is a power-amplified version of the switching pattern that switches between VPP and VNN. This signal is then low-pass filtered to obtain an amplified reproduction of the audio input signal. The processor portion of the TA3020 is operated from a 5-volt supply. In the generation of the switching patterns for the output MOSFETs, the processor inserts a "break-before-make" dead time between the turn-off of one transistor and the turn-on of the other in order to minimize shoot-through currents in the MOSFETs. The dead time can be programmed by setting the break-before-make control bits, BBM1 and BBM0. Feedback information from the output of the half-bridge is supplied to the processor via FBKOUT1. Additional feedback information to account for ground bounce is supplied via FBKGND1. The MOSFET drivers in the TA3020 are operated from

voltages obtained from VN10 and LO1COM for the lowside driver, and VBOOT1 and HO1COM for the high-side driver. VN10 must be a regulated 10V above VNN. N-Channel MOSFETs are used for both the top and bottom of the half bridge. The gate resistors, RG, are used to control MOSFET slew rate and thereby minimize voltage overshoots.

3.2.1.-Amplifier Gain**.** The gain of the TA3020 is the product of the input stage gain and the modulator gain. Please refer to the sections, Input Stage Design, and Modulator Feedback Design, for a complete explanation of how to determine the external component values.

$$AVTA3020 = AV\_INPUTSTAG * AV\_MODULATOR$$



Preamp and Amplifier Figure.

The gain of the input stage, above the low frequency high pass filter point, is that of a simple inverting amplifier:

$$AV_{INPUTSTAG} = -\frac{R13}{R9} = \frac{37.7k}{49.9k} = 0.7555$$

The modulator converts the signal from the input stage to the high-voltage output signal. The optimum gain of the modulator is determined from the maximum allowable feedback level for the modulator and maximum supply voltages for the power stage. Depending on the maximum supply voltage, the feedback ratio will need to be adjusted to maximize performance. The values of RFBA, RFBB and RFBC (see explanation below) define the gain of the modulator. Once these values are chosen, based on the maximum supply voltage, the gain of then modulator will be fixed even with as the supply voltage fluctuates due to current draw. shows how the feedback from the output of the amplifier is returned to the input of the modulator. The input to the modulator (FBKOUT1/FBKGND1 for

channel 1) can be viewed as inputs to an inverting differential amplifier. RFBA and RFBB bias the feedback signal to approximately 2.5V and RFBC scales the large R24/R21 signal to down to 4Vpp.

$$AVTA3020 \approx -\frac{R13}{R9} X (\frac{R21 * (R27 + R28)}{R27 * R28} + 1)$$

$$AVTA3020 \approx -19.123\, V/V$$

If the input voltage Vin in the TA3020 equal to 1.8V as this may be obtained through the microcontroller ATmega32 may modify the value of digital potentiometers.

$$VO_{TA3020} = 1.8 * -19.123 = -34.4214$$

$$P = \frac{VO_{TA3020}{}^{2}}{RS} = \frac{-34.4214\ ^{2}}{8\Omega} = 148.104W$$

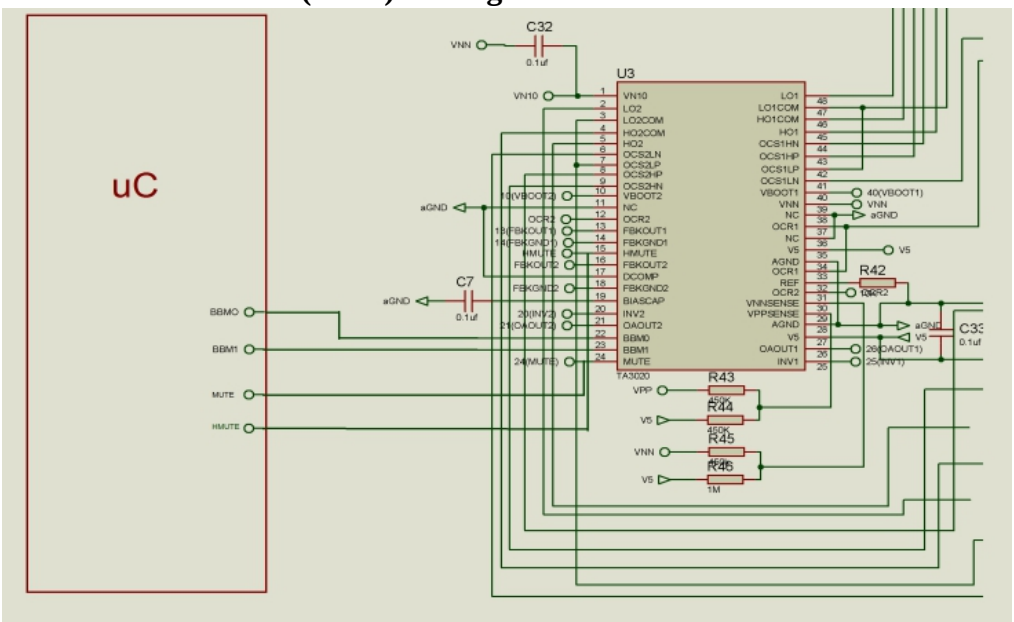
P is the power delivered by a single channel,

Overall serious p_t = 2 * P = 296.208W

If 4Ω load off you can get more power from p_t = 2 * 296,208 = 592.416W. MOSFETS supplies current so you can reach these powers are used. While it is true I clarify that if we want to generate more power MOSFETs we must increase depending on how much is required regarding the current required.

3.2.2.-TA3020 interaction with ATMEGA32uC Al igual que el TA1101B, el amplificador interactúa mediante pines de configuración. BM0, BM1 y periféricos MUTE, HMUTE.

Break-Before-Make (BBM) Timing Control



The half-bridge power MOSFETs require a deadtime between when one transistor is turned off and the other is turned on (break-before-make) in order to minimize shoot through currents. BBM0 and BBM1 are logic inputs (connected to logic high or pulled down to logic low) that control the break-before-make timing of the output transistors according to the following table.

BM1	BM0	DELAY
0	0	120ns
0	1	80ns
1	0	40ns
1	1	0ns

The tradeoff involved in making this setting is that as the delay is reduced, distortion levels improve but shootthrough, BBM1 should be grounded in most applications. All typical curves and performance information was done with using the 80ns or 120ns BBM setting. The actual amount of BBM required is dependent upon other component values and circuit board layout, the value selected should be verified in the actual application circuit/board. It should also be verified under maximum temperature and power conditions since shoot-through in the output MOSFETs can increase under these conditions, possibly requiring a higher BBM setting than at room temperature.

MUTE. When a logic high signal is supplied to MUTE, both amplifier channels are muted (both high- and low-side transistors are turned off). When a logic level low is supplied to MUTE, both amplifiers are fully operational. There is a delay of approximately 200 milliseconds between the de-assertion of MUTE and the un-muting of the TA3020.

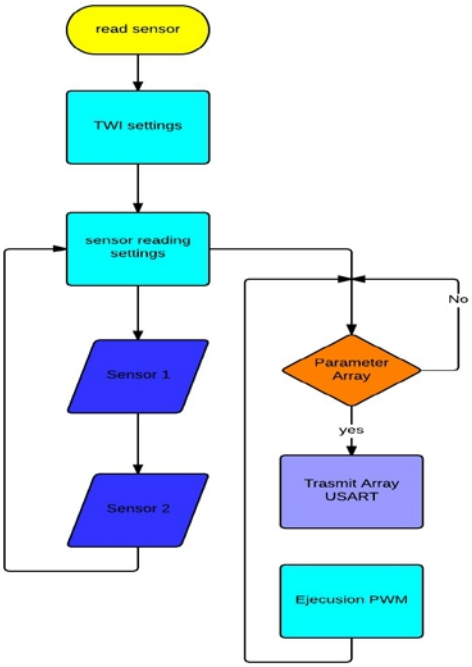
HMUTE. This is connected like input at uC.

The HMUTE pin is a 5V logic output that indicates various fault conditions within the device. These conditions include: over-current, overvoltage and undervoltage.

4. Control Circuit. As discussed previously we will use a programmable integrated circuit. In this step, an 8-bit microcontroller of undertaking various processes through scheduling algorithms. We can say that therefore the maximum use applications and modules offered by the uC. In this case we use the ATmega32 AVR. Is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega32 achieves throughputs approaching 1 MIPS per MHz Allowing the system designer to optimize power consumption versus processing speed. Significantly, we used Bus Interfaces ADC, I2C, PWM, USART, INT and I/O.

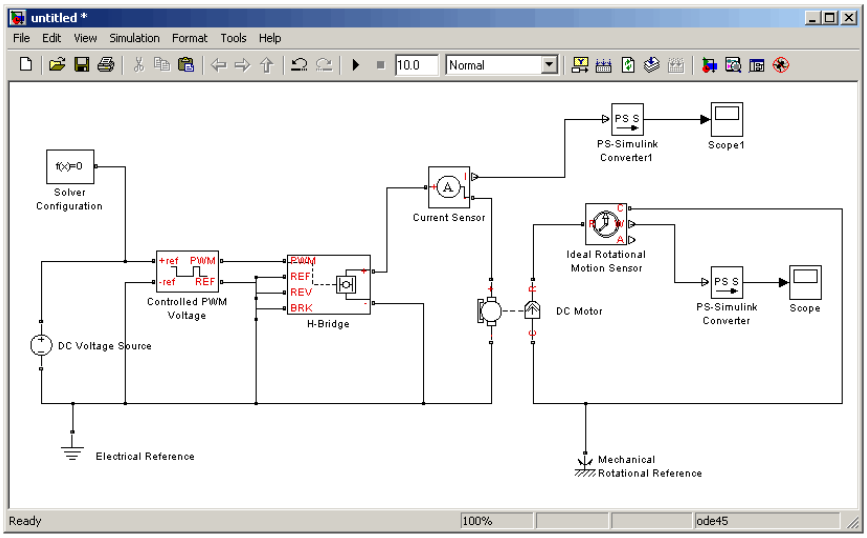
4.1- Detail Process Microcontroller. At this stage be explain the process and actions that will do the microonrolador. Through a series of programmed instructions. This process is divided equally by each stage of design, but in general for all programming is a control circuit that it must endure. First to start the uC makes a series of readings by the ADC module this must be because these parameters can identify if a and a signal at both entrances of the preamplifier, so it makes reading the ADC in the DC / DC converter Similarly happens with readings of two current sensors which is ACS712ELCTR. these readings are our essential input data. apart from that the USART is implemented to transmit the readings array.

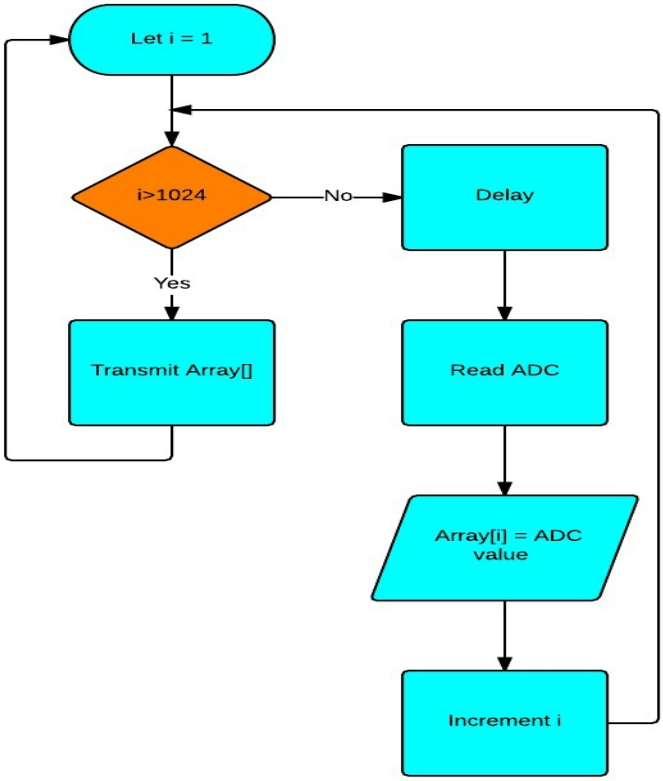
The action to executed through parameters reading in the ADC is a series of different processes and spread over the two first stages. This performs actions as modify AD5220BN100 digital potentiometers and modify the frequency of TIMER1A and TIMER1B, belonging to ATmega32, controlling the pulse width (PWM) found in the Buck-Boost.



Readings of protocol I2C / TWI, through this protocol the uC communicates with temperature sensors be found with power amplifiers. The monitoring system in which the temperature gradients of each sensor is obtained. If it will be compared the values of reading and then will be sent by the USART port, once that do this would be modified the PWM. The cooling system is implemented with three fans that are responsible of cooling the amplification circuits, these fans are controlled by PWM using

the TIMER0 of ATmega32 and are actuate the other two through trigger pulses every 100ms.





Set the Controlled PWM Voltage block parameters as follows:

PWM frequency = 4000

Simulation mode = Averaged

This value tells the block to generate an output signal whose value is the average value of the PWM signal. Simulating the motor with an averaged signal estimates the motor behavior in the presence of a PWM signal. To validate this approximation, use value of PWM for this parameter

Conclusion

Both analysis and theoretical control simulation showed that the use of a good control configuration based on energy regulation and switching amplifiers allows the temperature was controlling with excellent accuracy and reduces wear on stage of electronic circuit.

Acknowledgments

We thank staff Department of Electrical and Electronic, School of Mechanical and Electrical Engineering, University San Luis Gonzaga, Peru

Author contributions

Danilo Caceres Quintanilla, MSc. (Proffesor Associate Professor at the Department of Electrical and Electronic, School of Mechanical and Electrical Engineering, University San Luis Gonzaga, Peru).

References:

Cirrus Logic. (2015). Low Power Class-D Audio Amplifiers. Retrieved from https://www.cirrus.com/en/products/cs35l00-01-03.html

Crown International. (2001). Guia de aplicacion para amplificadores. Retrieved from http://www.crownaudio.com/media/pdf/135045.pdf

exas Instruments. (2014). Arbona J. PurePath Smart Amp Overview. Application Report. Retrieved from http://www.ti.com/lit/an/slaa625c/slaa625c.pdf

Zorzano, A.M. (2010). Amplificador de audio de alta fidelidad para sistemas activos de altavoces con bajo consumo de energía (Doctoral dissertation). Retrieved from Universidad La Rioja http://dialnet.unirioja.es/descarga/tesis/20788.pdf