A Novel Design and Implementation of 8-3 Encoder Using Quantum-dot Cellular Automata (QCA) Technology

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Abstract

In recent years Quantum-dot Cellular Automata (QCA) has been considered one of the emerging nano-technology for future generation digital circuits and systems. QCA technology is a promising alternative to Complementary Metal Oxide Semiconductor (CMOS) technology. Thus, QCA offers a novel electronics paradigm for information processing and communication system. It has attractive features such as faster speed, higher scale integration, higher switching frequency, smaller size and low power consumption compared to the transistor based technology. It is projected as a promising nanotechnology for future Integrated Circuits (ICs). A quantum dot cellular automaton complex gate is composed from simple 3-input majority gate. In this paper, a 8-3 encoder circuit is proposed based on QCA logic gates: the 4-input Majority Voter (MV) OR gate. This 7-input gate can be configured into many useful gate structures such as a 4-input AND gate, a 4-input OR gate, 2-input AND and 2-input OR gates, 2-input complex gates, multi-input complex gates. The proposed circuit has a promising future in the area of nano-computing information processing system and can be stimulated with higher digital applications in QCA.

Keywords: Quantum-dot Cellular Automata (QCA), Majority Voter (MV) Gate, QCA Logic Gates, QCA Designer, 8-3 Encoder Circuit

Introduction

Application of quantum technology in various fields is increasing day by day (Lent et al. 1993). In course of such a trend quantum-dot cellular automata are getting projected as a promising nanotechnology for future ICs (Lent, C. S., 1997). Recently, reversible (Bahar, et al., 2013; Sarker, et al.,

2014; Islam, et al. 2014 ; Shafi, et al. 2015; Islam, et al. 2016 ; Al-Shafi, et al. 2016) and (Abdullah-Al-Shafi, M., 2016) circuits have been implemented in QCA by the researchers successfully. A QCA is an array of structures known as quantum-dots. Computing with QCA is achieved by the tunneling of individual electrons among the quantum-dots inside a cell and the classical coulombic interaction among them. A quantum cell can be viewed as a set of four charge containers or dots positioned at the corners of a square, as shown in Fig. 1. It contains two extra mobile electrons. The electrons can quantum mechanically tunnel between dots but cannot come out from the cell and are forced to settle at the corner positions due to coulomb interaction. Thus, there exist two equivalent energetically minimal arrangements for the electrons in a QCA cell.

In Fig. 1, a QCA cell and its binary logic are shown. The energetically position of the diagonal electrons identify the binary logic 0 or 1. This phenomenon is useful in nanotechnology which affects high resolution fast electronic circuits.

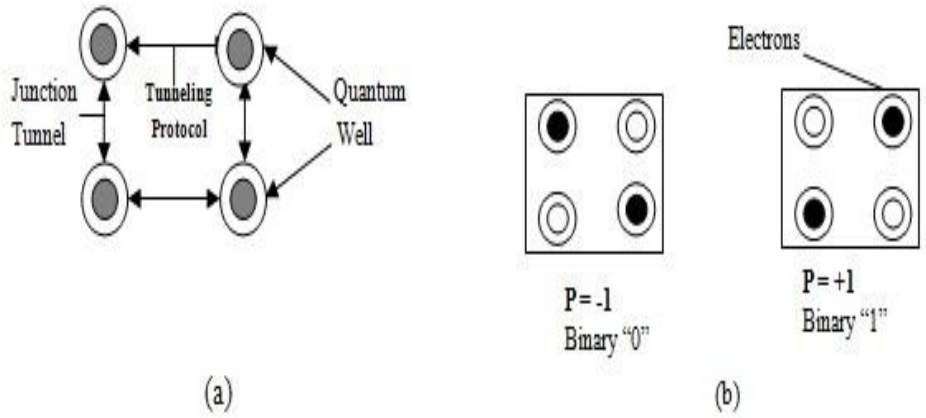

Fig.1. A QCA cell and its binary logic, (a) Structure of a QCA cell, (b) Representing a binary digit with the help of 2 different polarizations of the localized electron

QCA Wires

The QCA cells themselves comprise the interconnecting wires (Lent et al. 1993). QCA cells are described in (Niemier, M. T., A. F. Rodrigues and P. M. Kogge., 2002) . An example of a QCA wire is shown in Figure 2. In this example, a value of 1 is transmitted along the wire. Only a slight polarization in a cell is required to fully polarize its neighbor. The direction for the flow of information through a gate or a wire is controlled by a four stage clocking system which raises and lowers barriers between the cells (Lent, C. S., et al 1997).

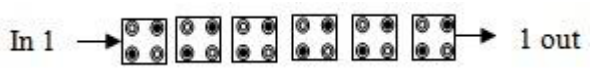

Fig. 2. QCA wire

QCA Logic Gates

The fundamental logic gate for QCA is a 3-input majority gate which consists of five cells. Three of those cells accept three inputs to the cell, labeled as ‘a’, ‘b’, and ‘c’. The center cell is the device cell which performs the calculation. The remaining cell, labeled out, provides the output. The circuit shown in Figure 3 performs the Boolean function, out = ab + bc + ca.

Truth Table

A	B	C	MV (A,3, C)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

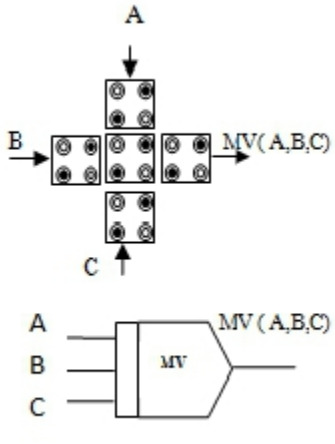

Fig. 3. Three-input majority gate

Described in (Lent et al. 1994) were other logic gates formed by restricting the polarity of one input to the 3-input majority gate to be a constant value. Figure 4 illustrates a 2-input AND gate and a 2-input OR gate formed in this manner. By replacing input c with a cell having a fixed polarity of 0, the 3-input majority gate functions as an AND gate. In the example of AND gate on the left side of Figure 4, out = a,b. Similarly, replacing input c with a cell having a fixed polarity of 1 creates a 2-input OR gate. In the example of OR gate on the right side of Figure 4, out = a+b.

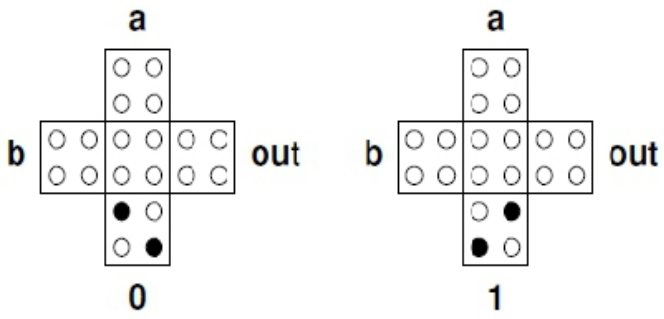

Fig.4. Two-input AND and Two-input OR gates

Input Complex Gates

Despite that the fundamental logic structure of QCA is the 3-input majority gate, many of the attempts to implement functional circuitry using these majority gates begin by restricting them to a subset of their full information content potential. Previous complex gates, requiring more than one device cell are described in the literature; however these complex gates are still restricted to implementing 2- input functions. In (Niemier, M. T., A. F. Rodrigues and P. M. Kogge., 2002) a complex gate is used to implement a 2-input XOR function (Bahar, et al. 2017). In (Bahniman et al. 2013) a 3-input majority gate restricted to an AND gate configuration (similar to that shown in Figure 4) followed by an inverter was used to form 2-input NAND building blocks for an FPGA implementation. An alternative to this approach however, is to use the 3-input majority gate as a building block to build even larger and more complex gate components containing multiple control and information inputs.

Multi-input Complex Gates

Figure 5 shows a 7-input gate. This gate is composed of three 3-input majority gates. Three of the inputs to this gate are e; f; and g, function as control inputs that are used to specify the functionality of the circuit. The remaining four Inputs, a; b; c; and d, are used to implement Boolean functions of four variables. The functionality of this gate for all configurations has been simulated using QCA Designer (Walus, K. et al. 2004). Several of the more useful configurations for this complex gate are described in further detail within this section. In addition, reduced configurations are also discussed.

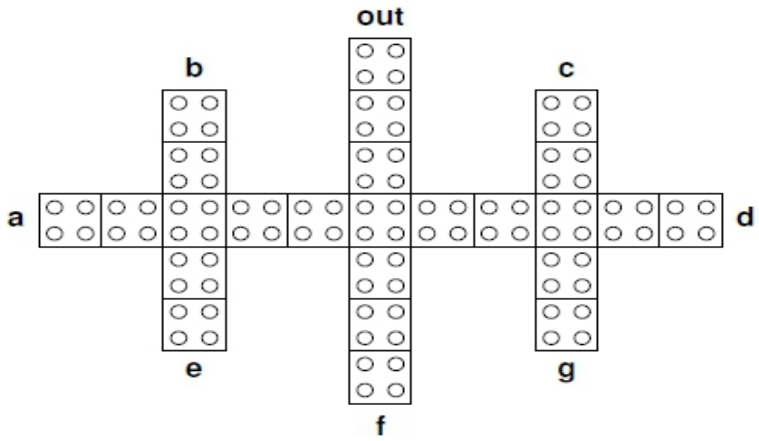

Fig. 5. Seven-input complex gate

Four-Input AND Gates

The 7-input gate of Figure 5 can be used to form a 4- input AND gate as shown in **Figure 6** by restricting inputs 'e', 'f' and 'g' to have a fixed polarity that is equal to 0. Although the selection of 'f' is unique, either 'a' or 'b' can be restricted rather than 'e' and similarly 'c' or 'd' can be selected for restriction rather than 'g'. For the example of circuit as shown in Figure 6, the function represented is out = a,b,c,d.

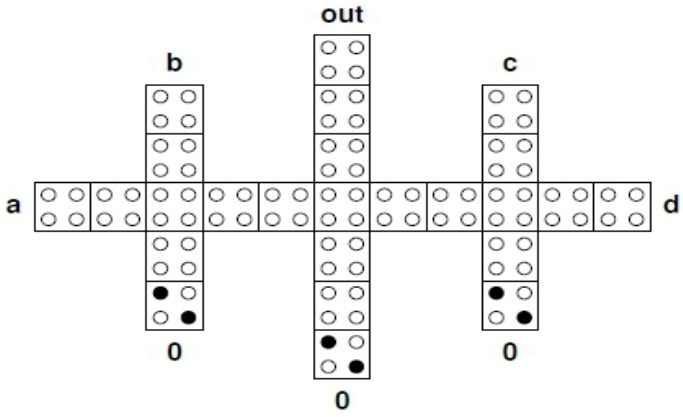

Fig. 6. Four-input AND gate

Four-Input OR Gates

Similarly, the 7-input gate of Figure 5 can also be used to form a 4-input OR gate. For this configuration the inputs 'e', 'f' and 'g' are restricted to have a fixed polarity that is equal to 1. As for the AND gate, the selection of 'f' is unique. For the remaining two fixed polarity cells, the same symmetry is presented in the OR gate as in previously described AND gate, either 'a' or 'b' can be restricted rather than 'e' and likewise 'c' or 'd' can be selected for restriction rather than g. The function represented is out = a + b + c + d.

Proposed 8-3 Encoder

In Traditional 8-3 encoder logic diagram is presented in Fig. 7.

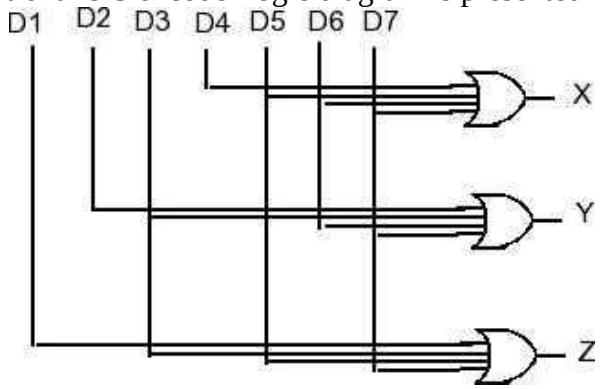

Fig. 7. Traditional 8-3 encoder logic diagram

The block diagram of QCA is the 8-3 encoder shown in **Figure 8**.

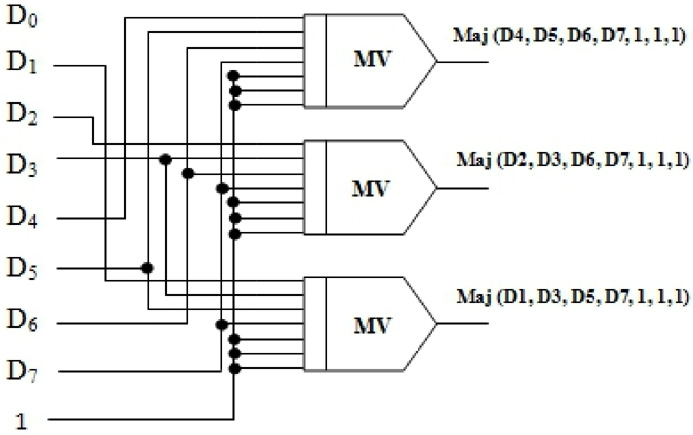

Fig. 8. Block Diagram of QCA is the 8-3 encoder.

The fundamental logic gate for QCA is the 8-3 encoder shown in **Figure 9** that is composed of Seventy Nine (79) cells. In general, an 8-3 encoder has an output expression as is shown in Eq. (1) where D_1, D_2, D_3, D_4, D_5, D_6, and D_7 are the seven inputs.

$$\begin{cases} X = D4, D5, D6, D7; \\ Y = D2, D3, D6, D7; \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1) \\ Z = D1, D3, D5, D7; \end{cases}$$

In Fig. 9, when the binary signals (0 and 1) are inputted into the 8-3 encoder circuit, the input digits (D_1 , D_2, D_3, D_4, D_5, D_6, D_7) are decoded to the decimal digits(X, Y, Z). According to the logic computation in Fig. 9, we can represent this logic expressions based on the majority gates as shown in Eq. (2).

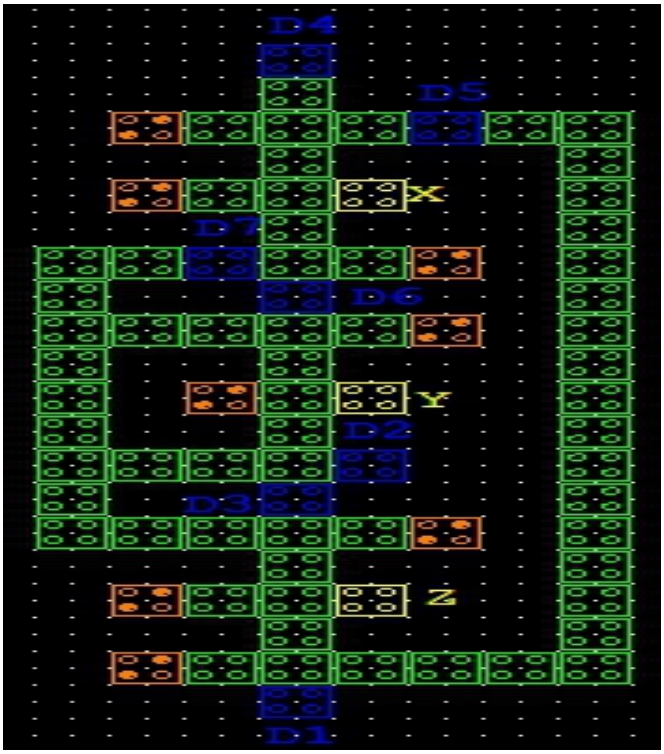

Fig. 9 QCA layout structure of 8-3 encoder

$$\begin{cases} X = MV(D4, D5, D6, D7, 1, 1, 1); \\ Y = MV(D2, D3, D6, D7, 1, 1, 1); \\ Z = MV(D1, D3, D5, D7, 1, 1, 1); \end{cases} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

So we find the results of X, Y, Z, fulfill the digital logic technology of 8-3 encoder circuit.

The 8-3 encoder circuit layout has been simulated using QCA Designer 2.0.3; a layout and simulation tool for QCA. The simulation results for an 8-3 encoder circuit are shown in Figure 10.

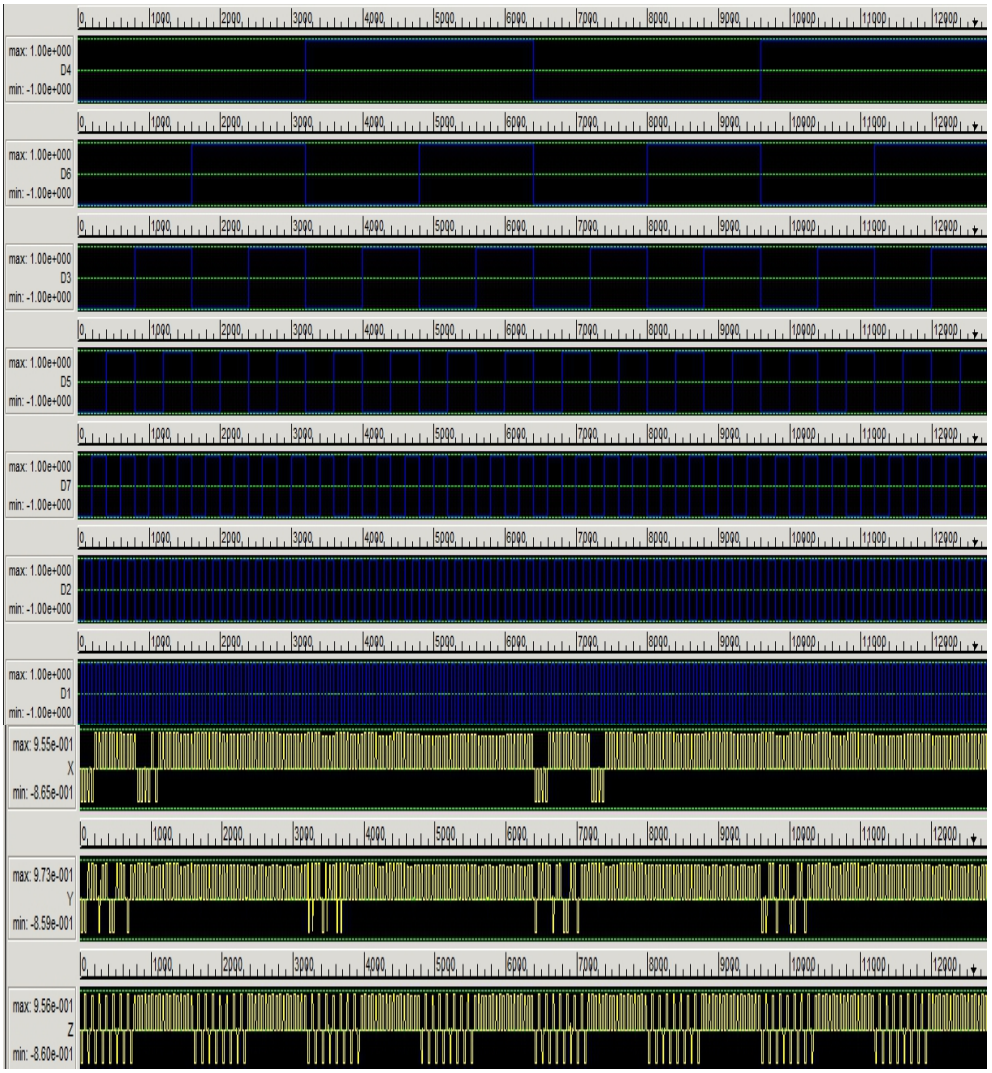

Fig.10 Simulated waveforms for 8-3 encoder circuit

In this Simulation we used the coherence vector computational engine and the following parameters: 10nm × 10nm cell size, 2.5nm cell-to-cell distance, and 2.5 dot size and 40nm radius of influence.

Table 1 Comparison of proposed designs

Design	Number of cells	Area (in μm^2)	Delay
8-3 bit simple encoder Bahar, A. N.	281	0.22 × 0.30 = 0.06	2.25
Proposed 8-3 bit simple encoder	79	0.32 × 0.42 = 0.13	1.25

Conclusions

This paper presents an 8-3 encoder that consists of 7-input majority gate. Three of these inputs typically function as control inputs to determine the Boolean function formed by the four other inputs to the circuit. This 7-input gate can be configured as a 4-input OR gate, a product of sums representation, a sum of products representation, and other variations. This QCA circuit design provides a new functional paradigm for information encoding. In addition, QCA binary logic functions and the associated new nano-technology will provide high-speed computing, high-density applications. It is believed that QCA will become a more practical way to create a faster and denser circuit. All designs are carefully clocked and functionally verified using QCAdesigner. Finally, in Table 1, designs are compared in terms of number of cells, area and delay.

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